

Regional Innovation Centre for Electrical Engineering
Univerzitni 26 306 14 Plzen Czech Republic

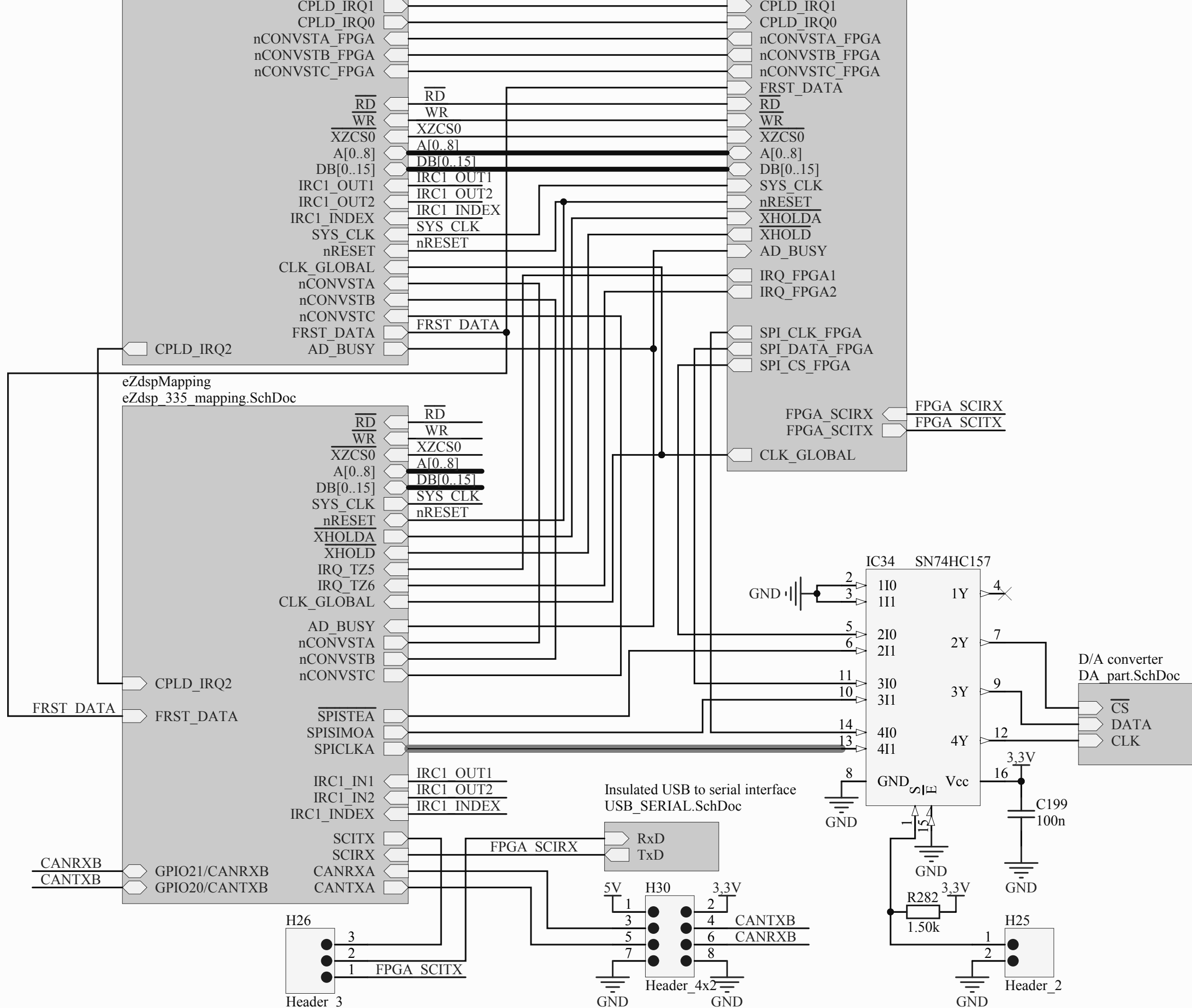
Size: A4
Date: 5.8.2014
Author: Tomáš Košan
Checked by: LiPo, MaJa
Approved by: Z. Peroutka

Title: SCH_title	
Subtitle: [SUBTITLE]	
Nr.: 1	Revision: 0.2
Type: typ	Sheet 1 of 1
File: PWM_level_shifter_6ch.SchDoc	

Note: Data in fields enter via project/document parameters.

CPLD_part.SchDoc
Address decoder and IO

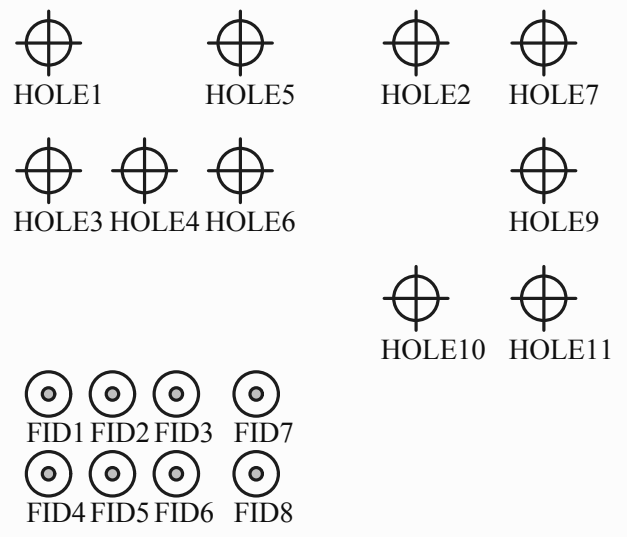
FPGA part
FPGA_part.SchDoc



Power source
power_source.SchDoc

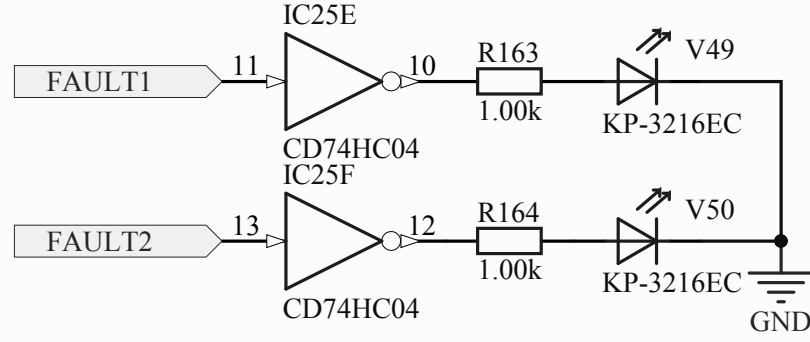
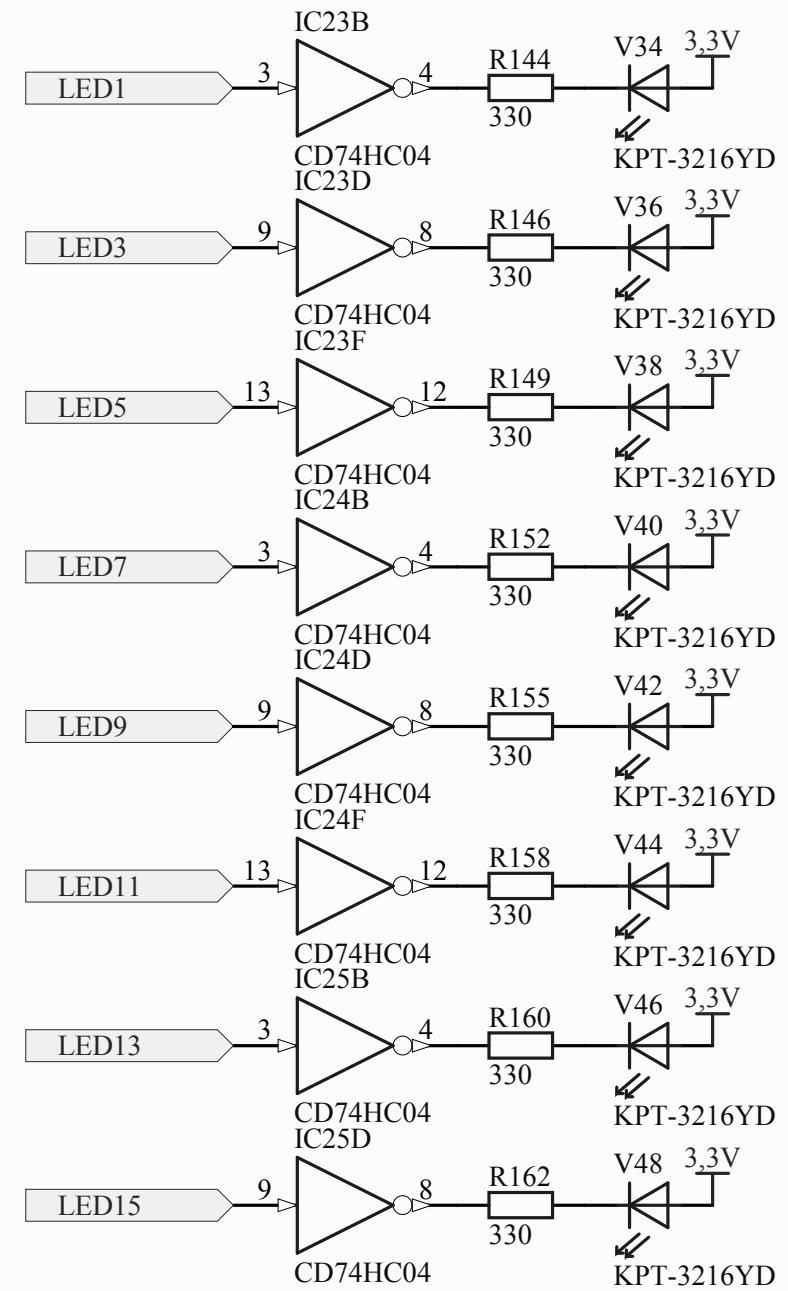
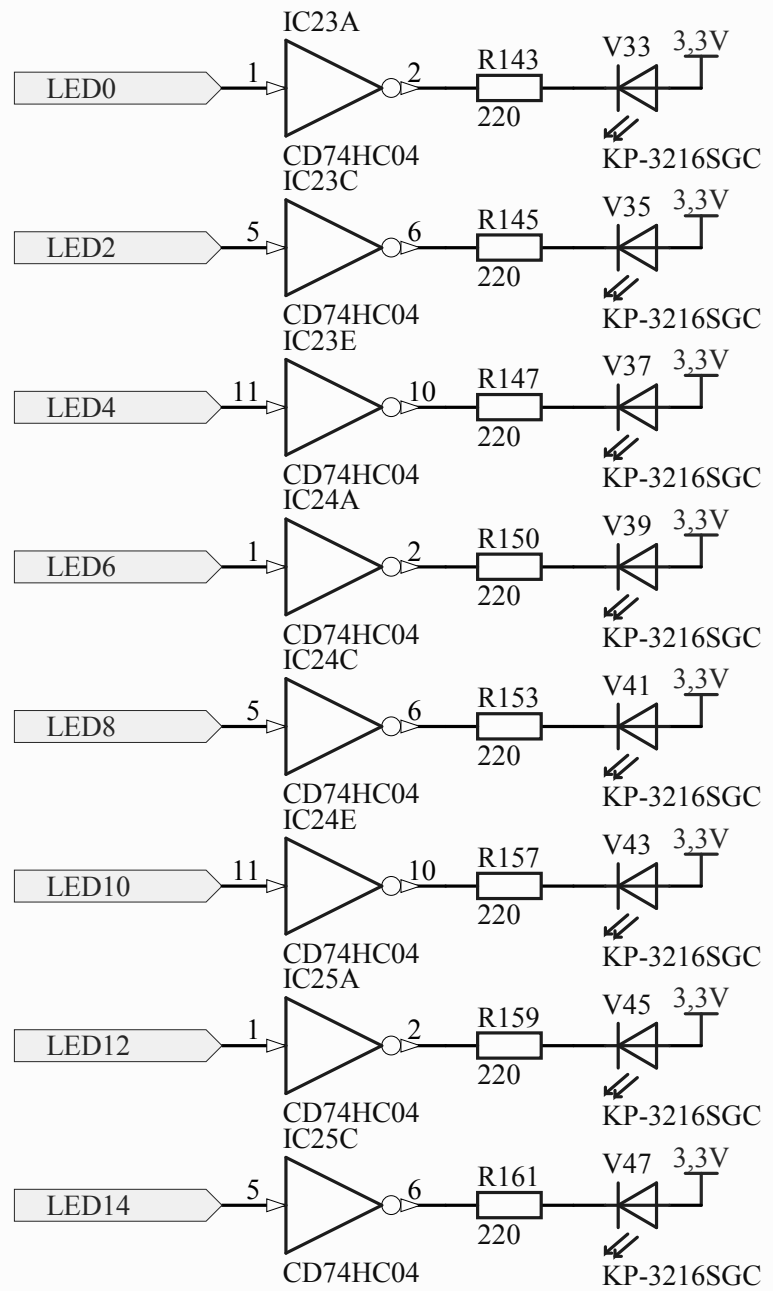
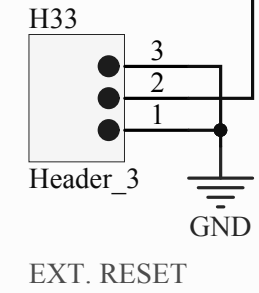
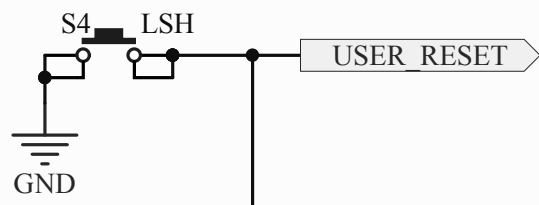
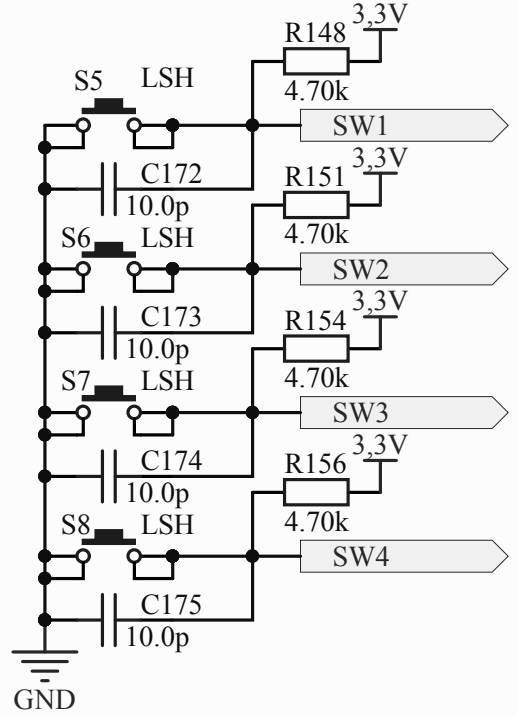
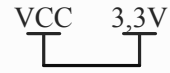
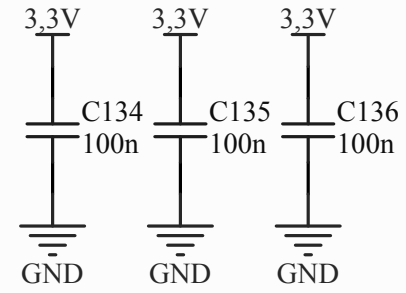
Power source FPGA
power_source_FPGA.SchDoc

Indicators
power_indicators.SchDoc



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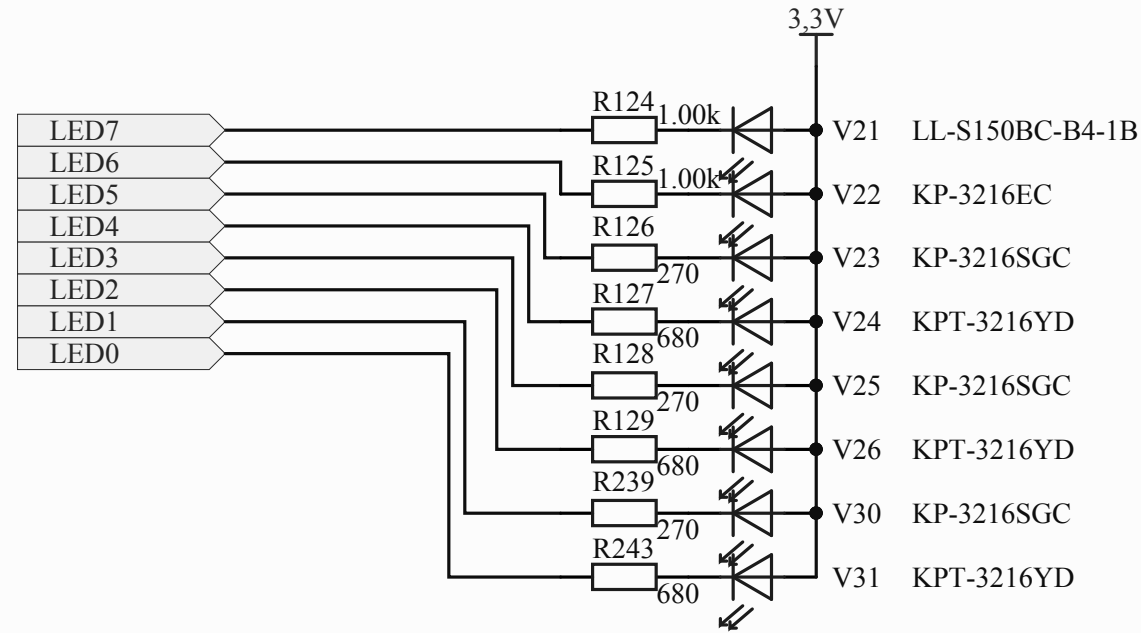
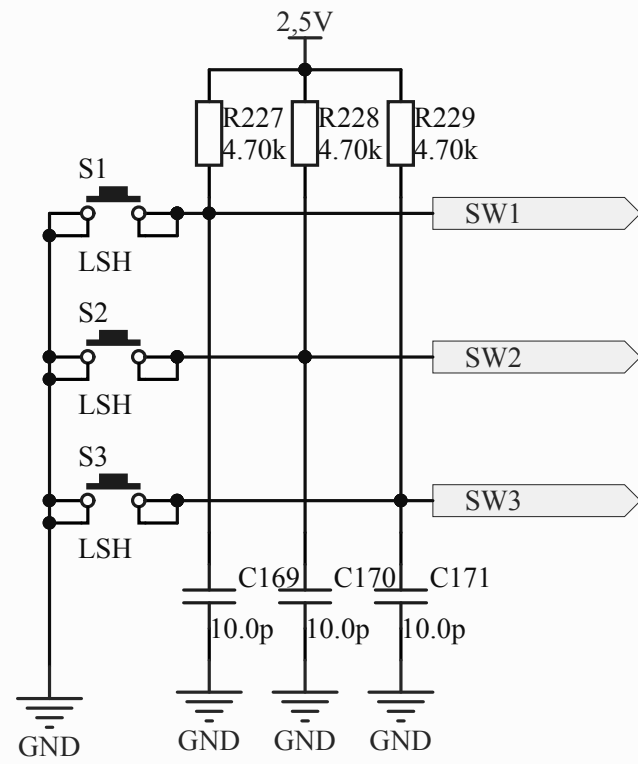
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Author: Tomáš Košan	Subtitle: [SUBTITLE]		
Checked by: LiPo, MaJa	Nr.: 1	Revision: 0.2	
Approved by: Z. Peroutka	Type: typ	Sheet 1 of 1	
File: Interface_card.SchDoc			



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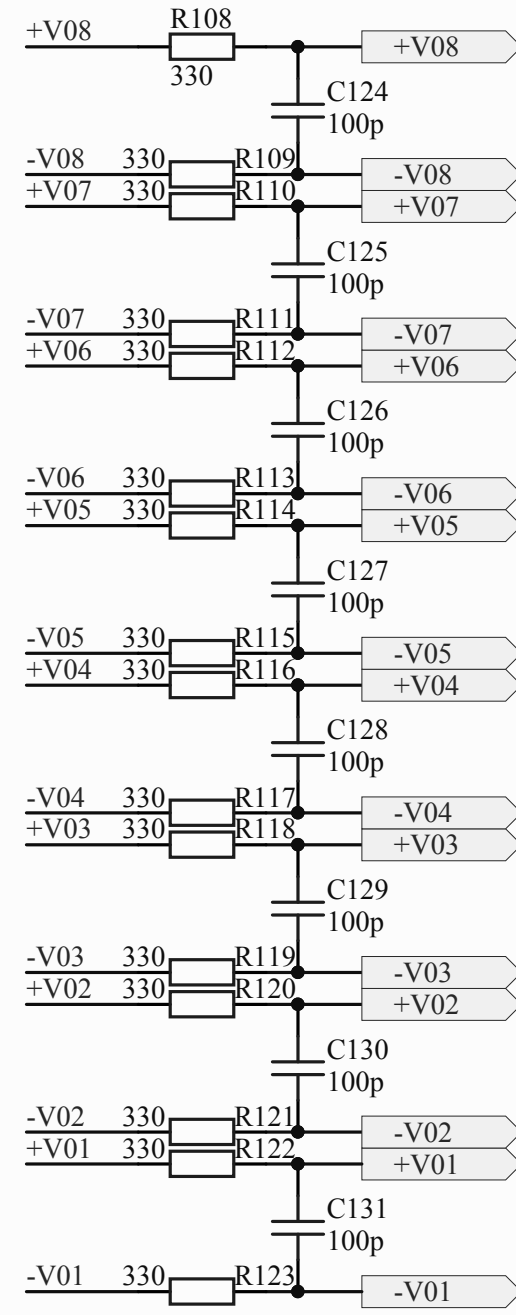
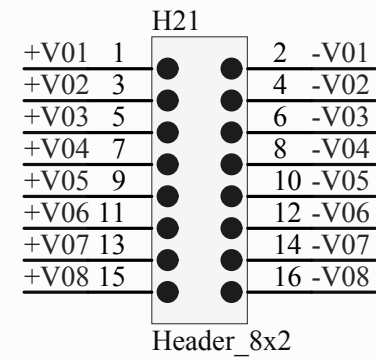
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Author: Tomáš Košan	Subtitle: [SUBTITLE]		
Checked by: LiPo, MaJa	Nr.: 1	Revision: 0.2	
Approved by: Z. Peroutka	Type: typ	Sheet 1 of 1	
File: UserInterfaceDSP.SchDoc			

Note: Data in fields enter via project/document parameters.



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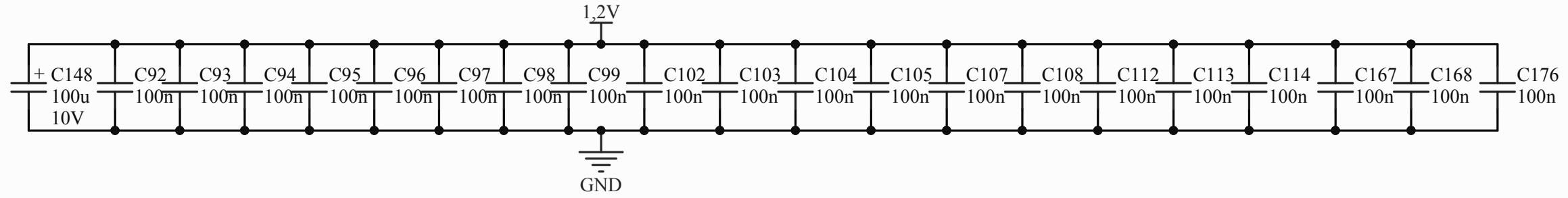
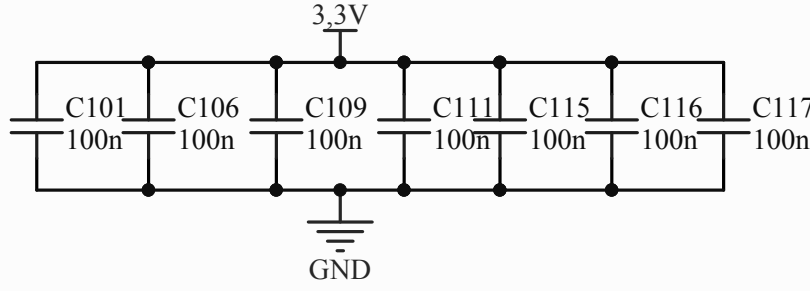
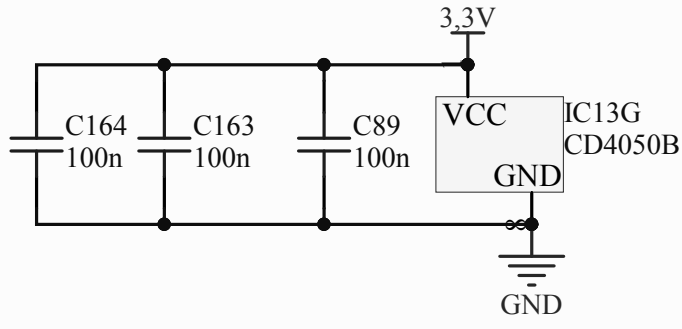
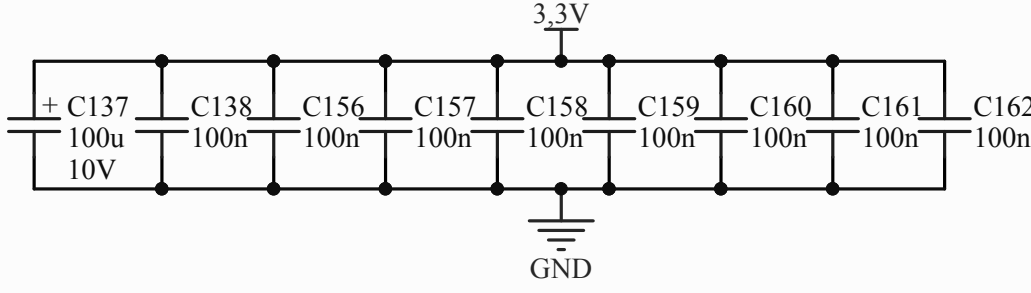
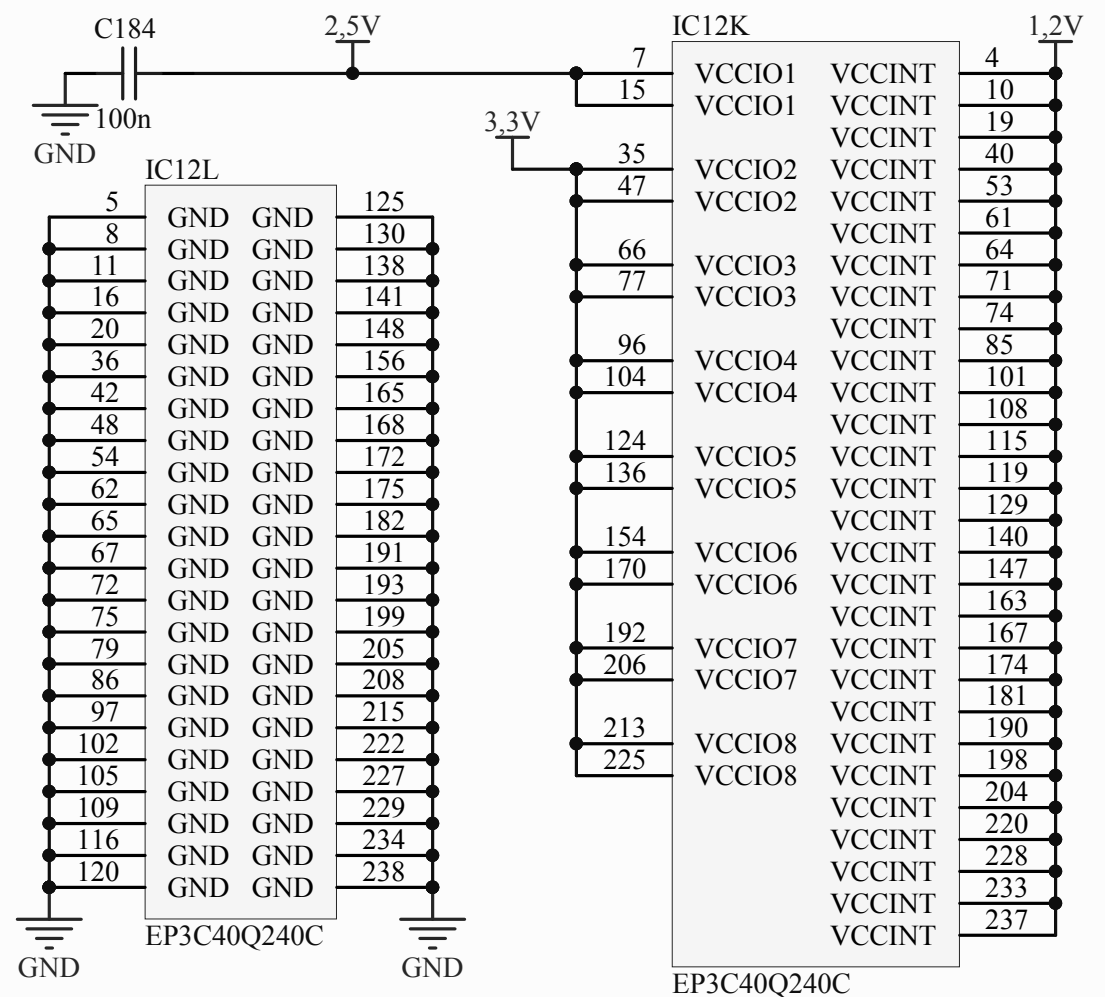
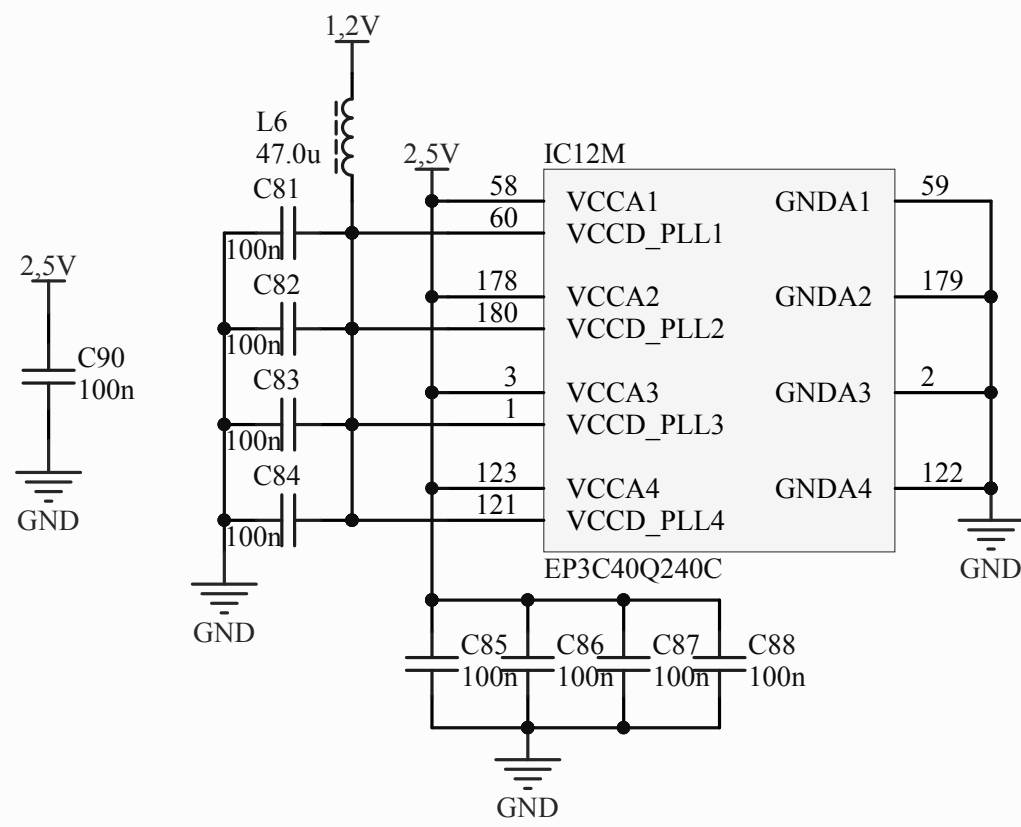
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Approved by: Z. Peroutka	Type: typ	Sheet 1 of 1	
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Size: A4	Date: 5.8.2014	Title: SCH_title	
Author: Tomáš Košan	Subtitle: [SUBTITLE]		
Checked by: LiPo, MaJa	Nr.: 1	Revision: 0.2	
Approved by: Z. Peroutka	Type: typ	Sheet 1 of 1	
File: AD_InputFilter.SchDoc			

Note: Data in fields enter via project/document parameters.



 Regional Innovation Centre for Electrical Engineering Univerzitni 26 306 14 Plzen Czech Republic	Size: A4	Date: 5.8.2014	Title: SCH_title	
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	Checked by: LiPo, MaJa	Nr.: 1	Revision: 0.2	
	Approved by: Z. Peroutka	Type: typ	Sheet 1 of 1	
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A

A

B

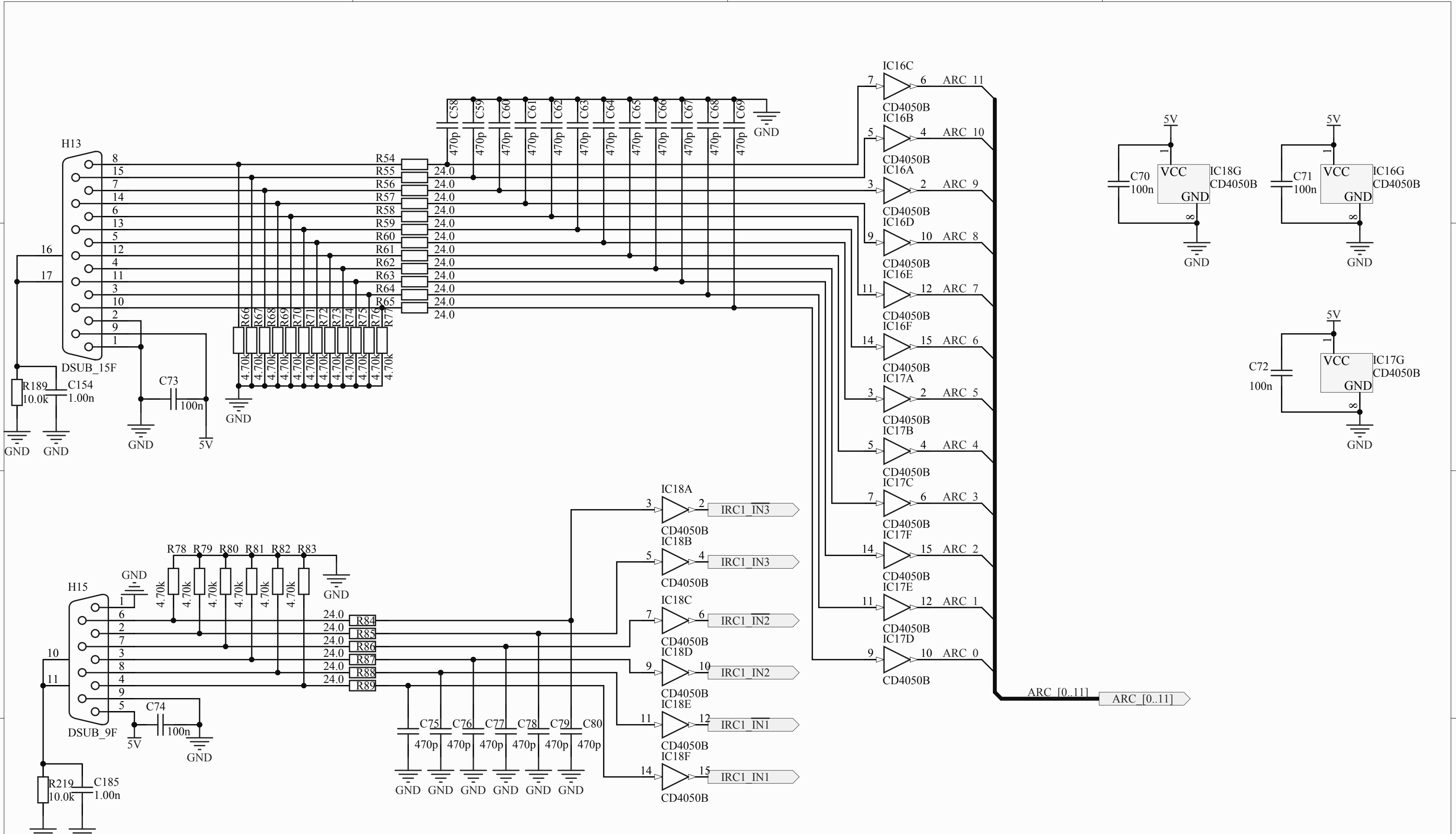
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C

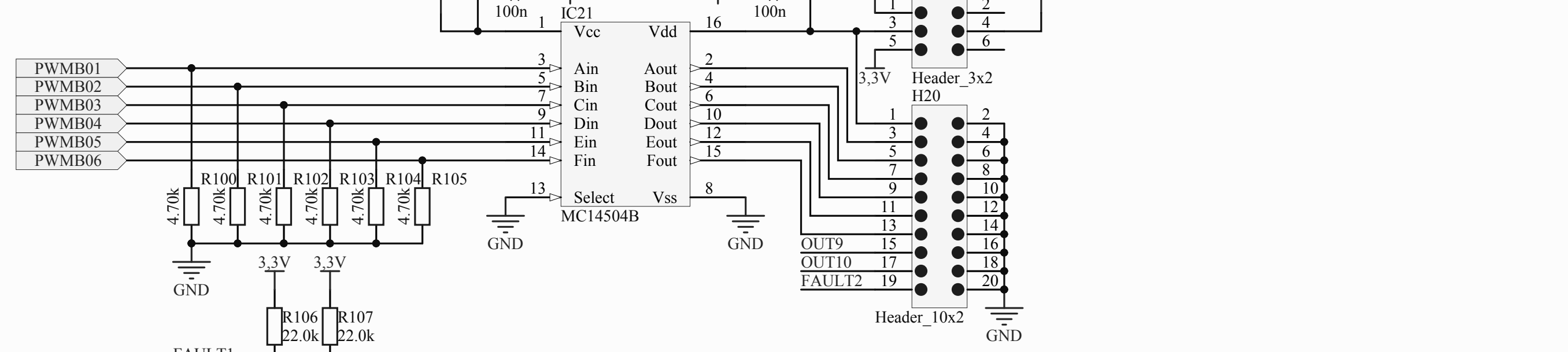
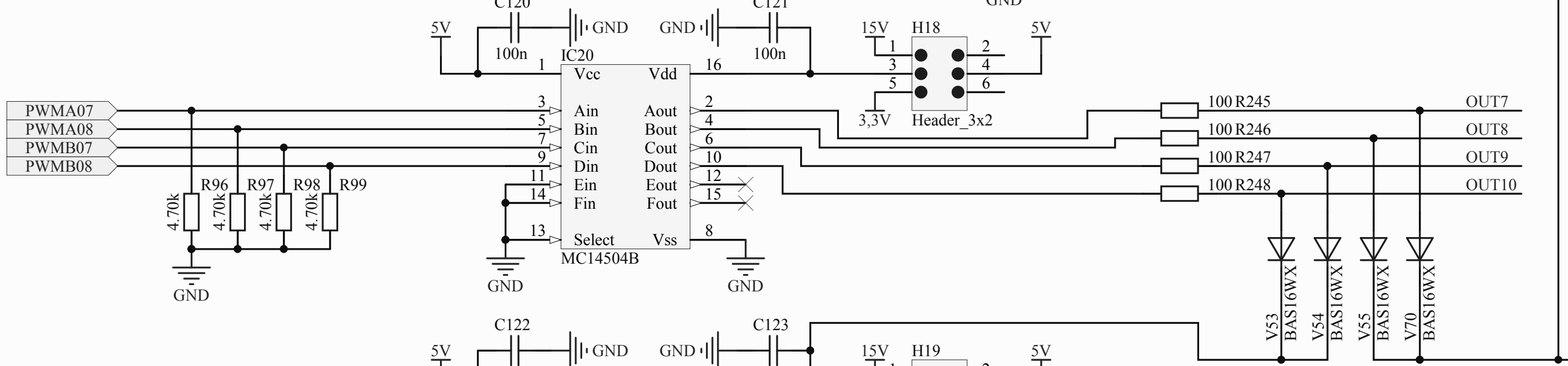
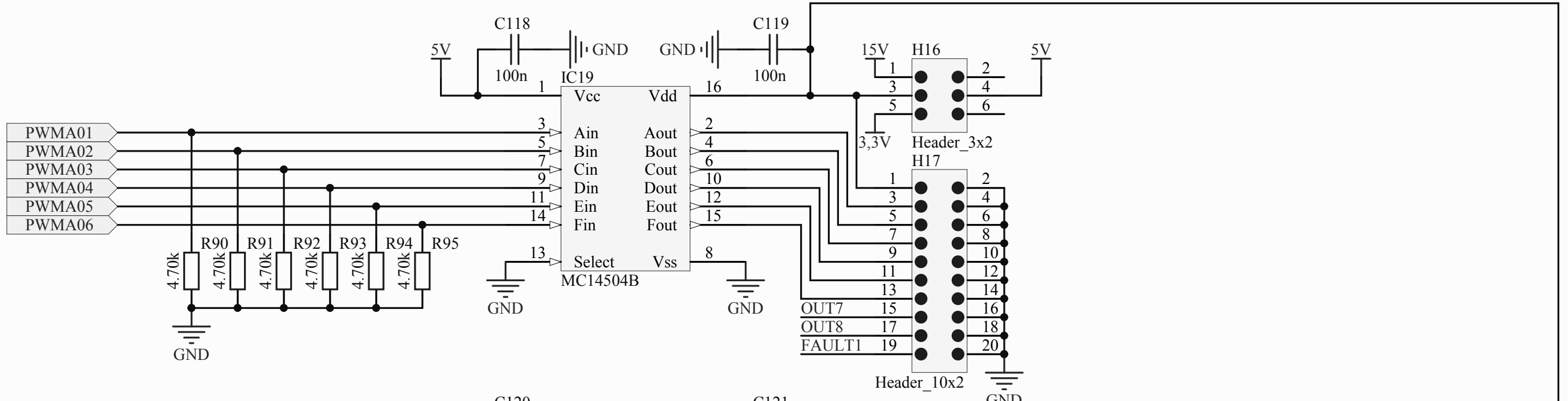
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D

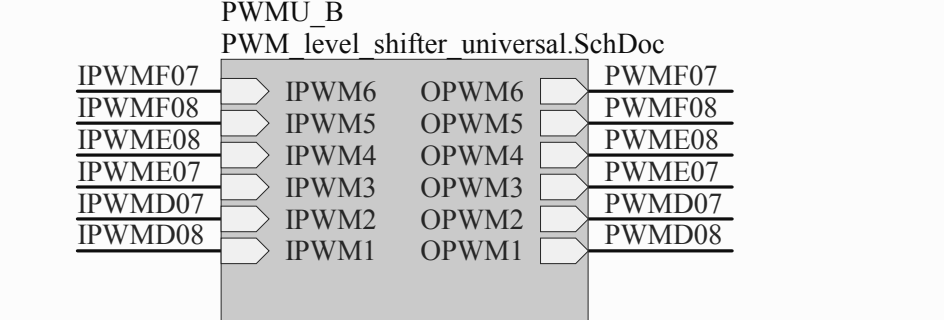
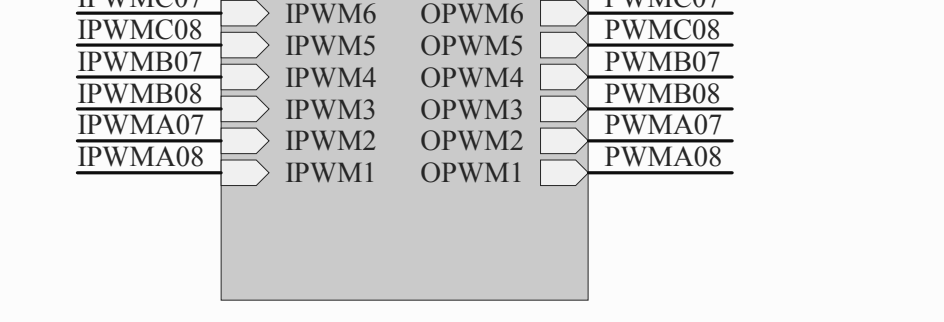
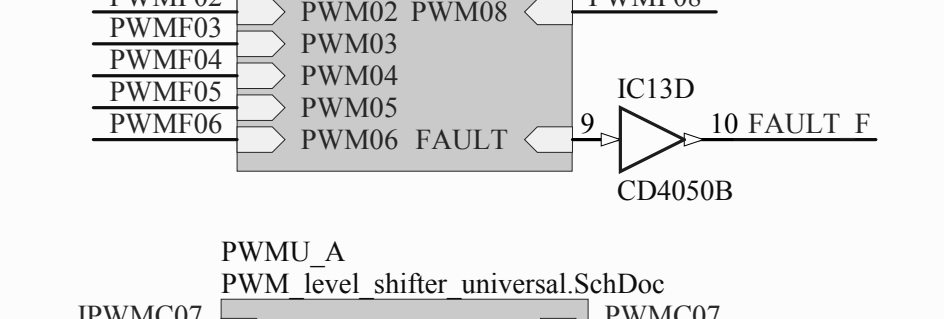
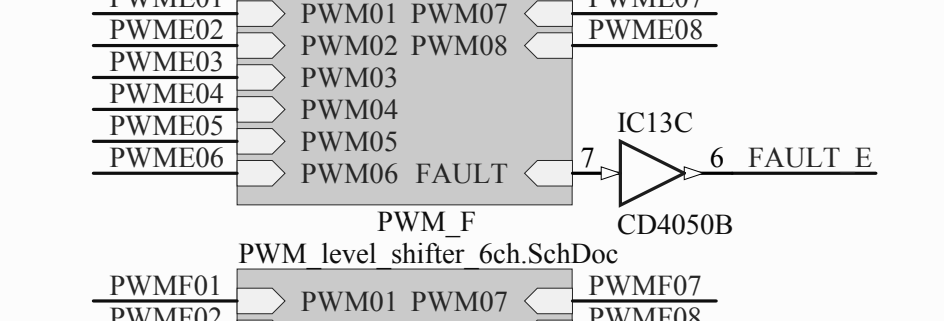
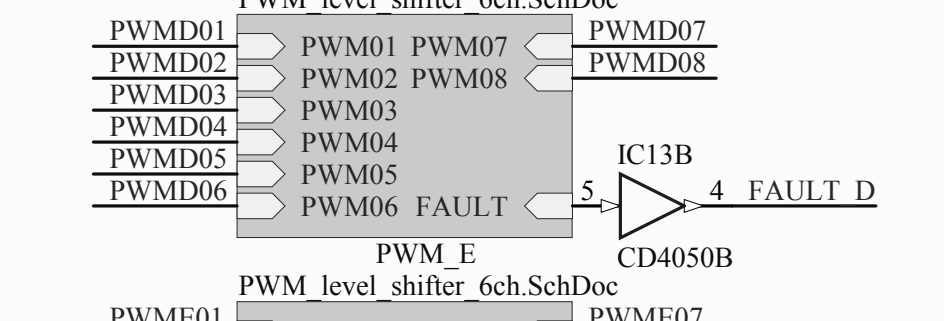
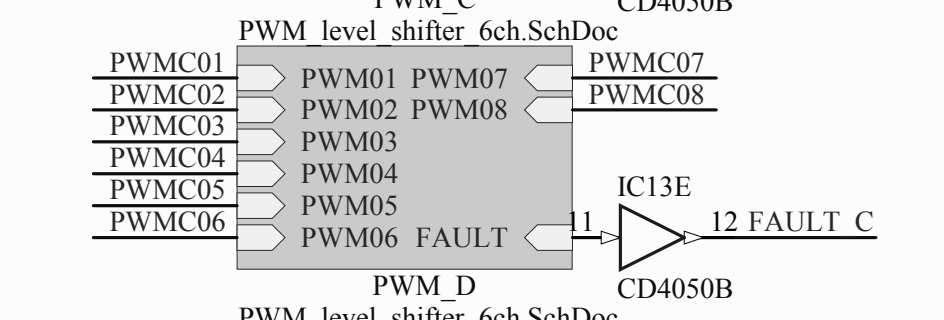
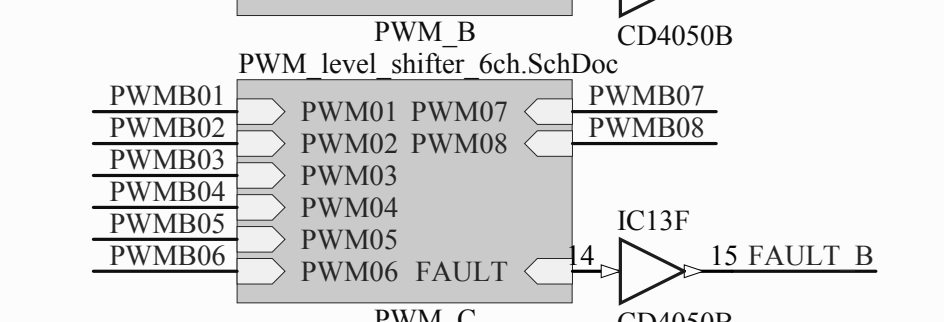
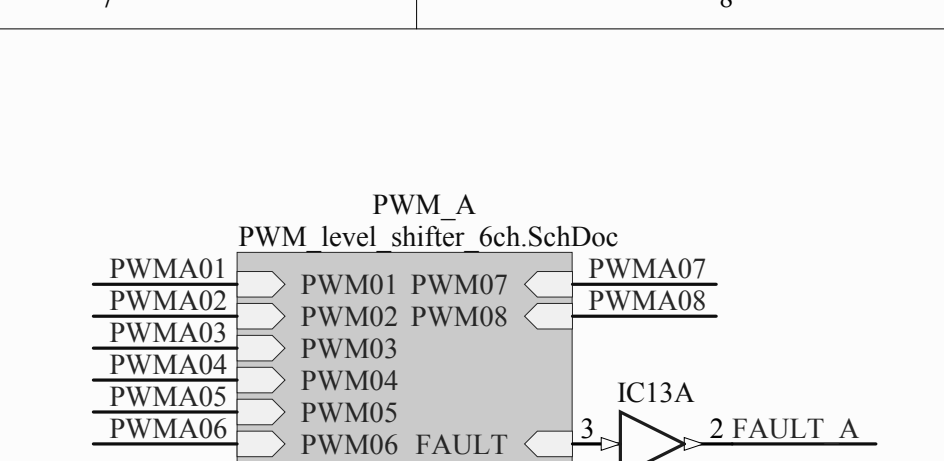
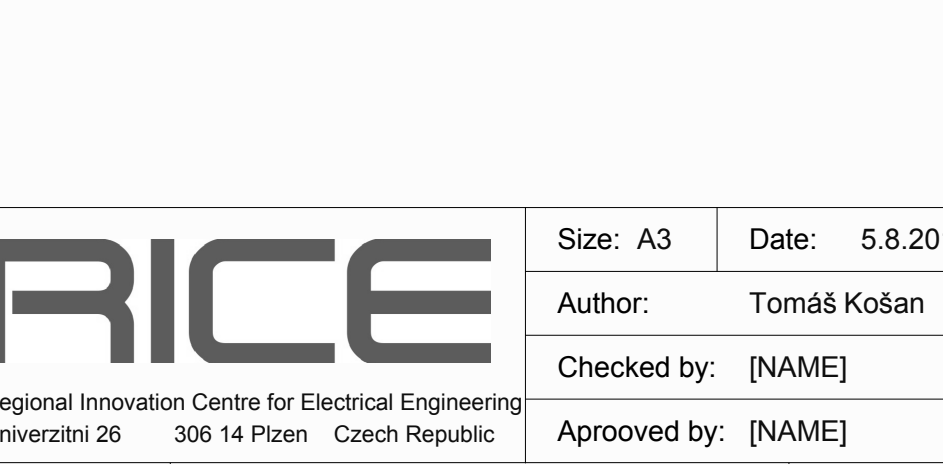
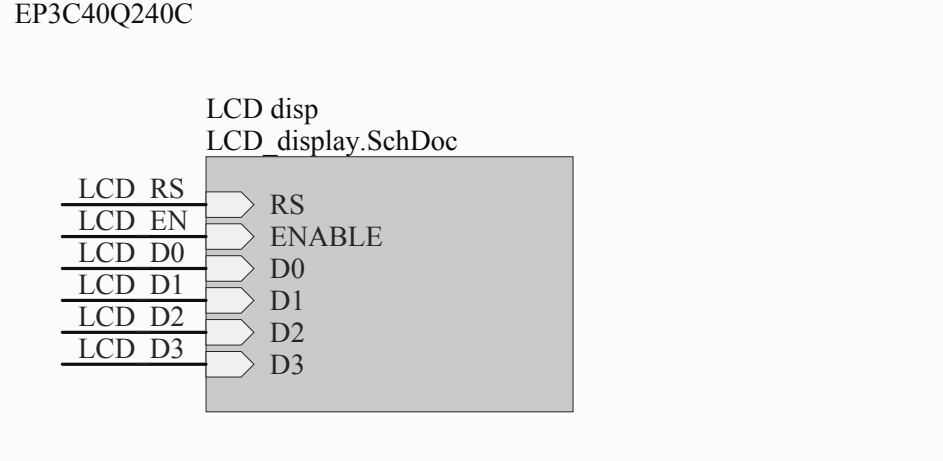
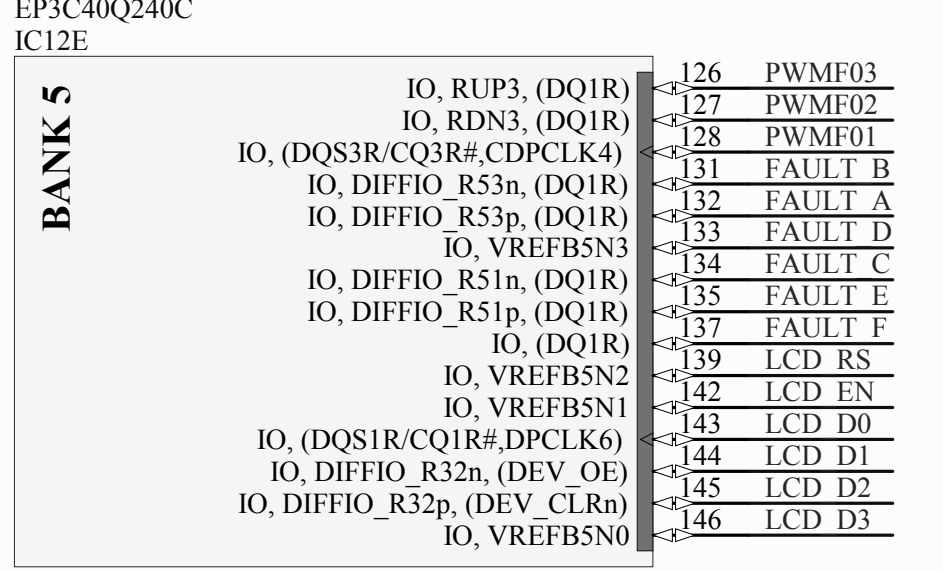
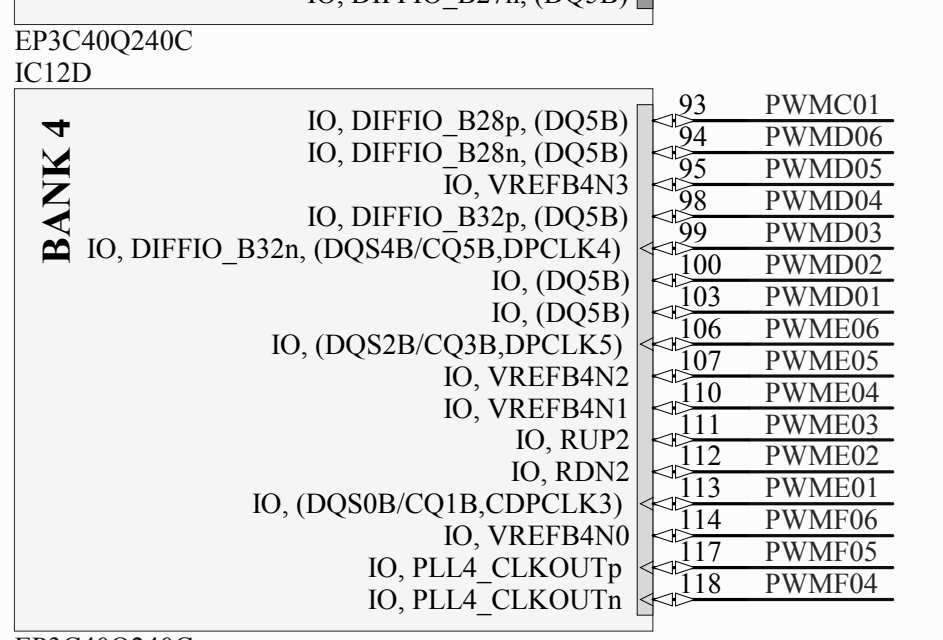
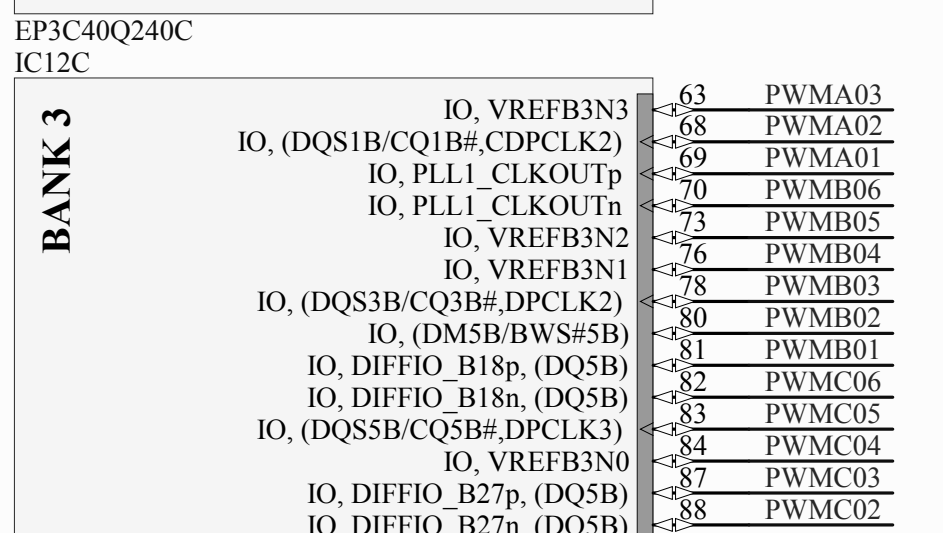
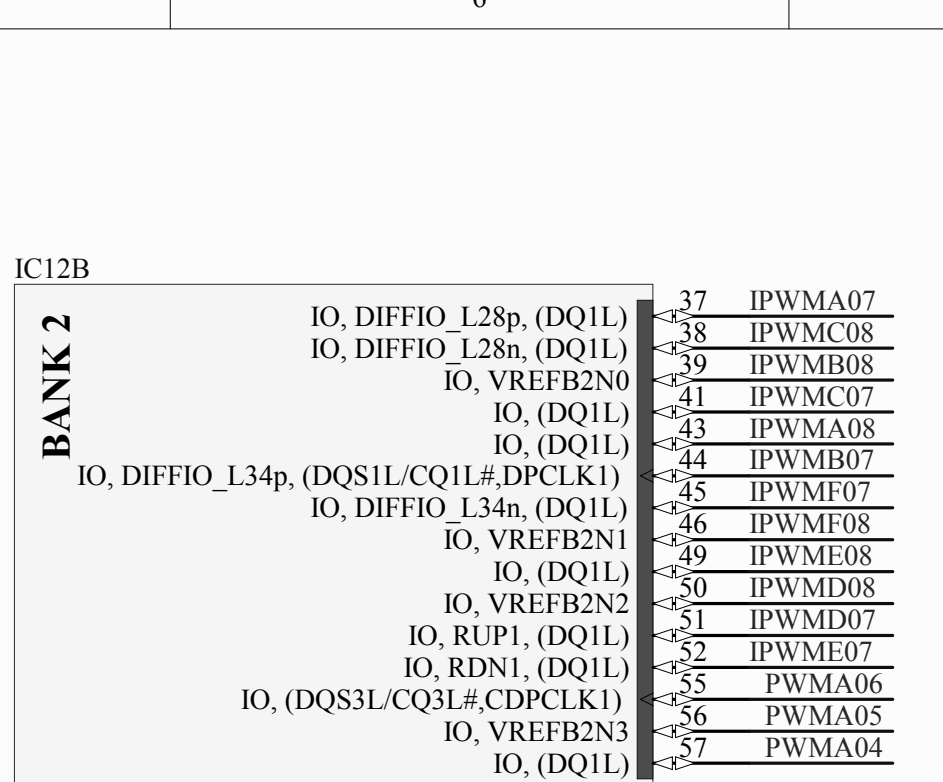
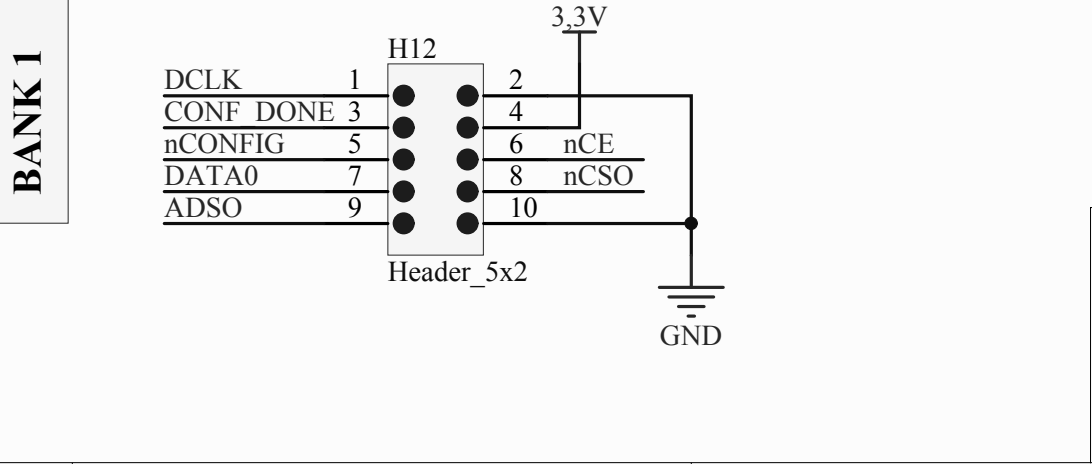
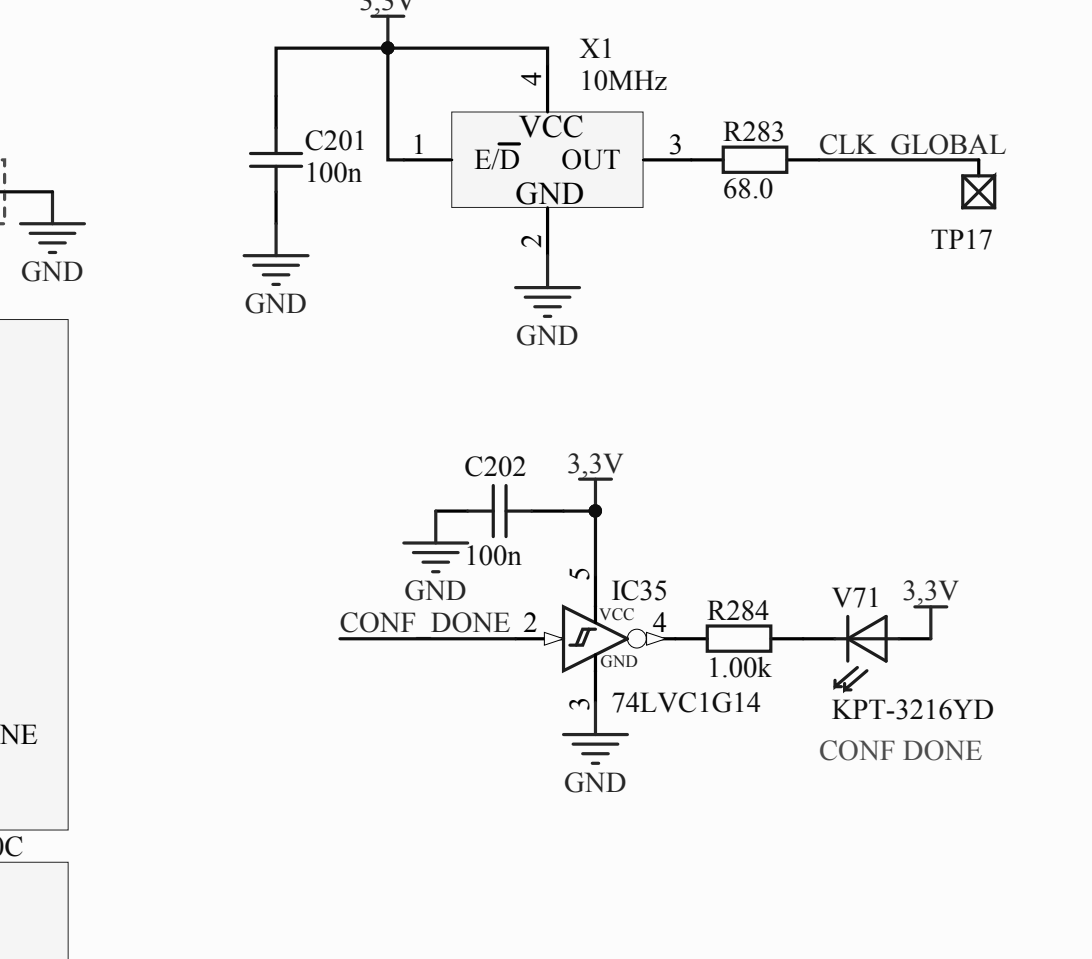
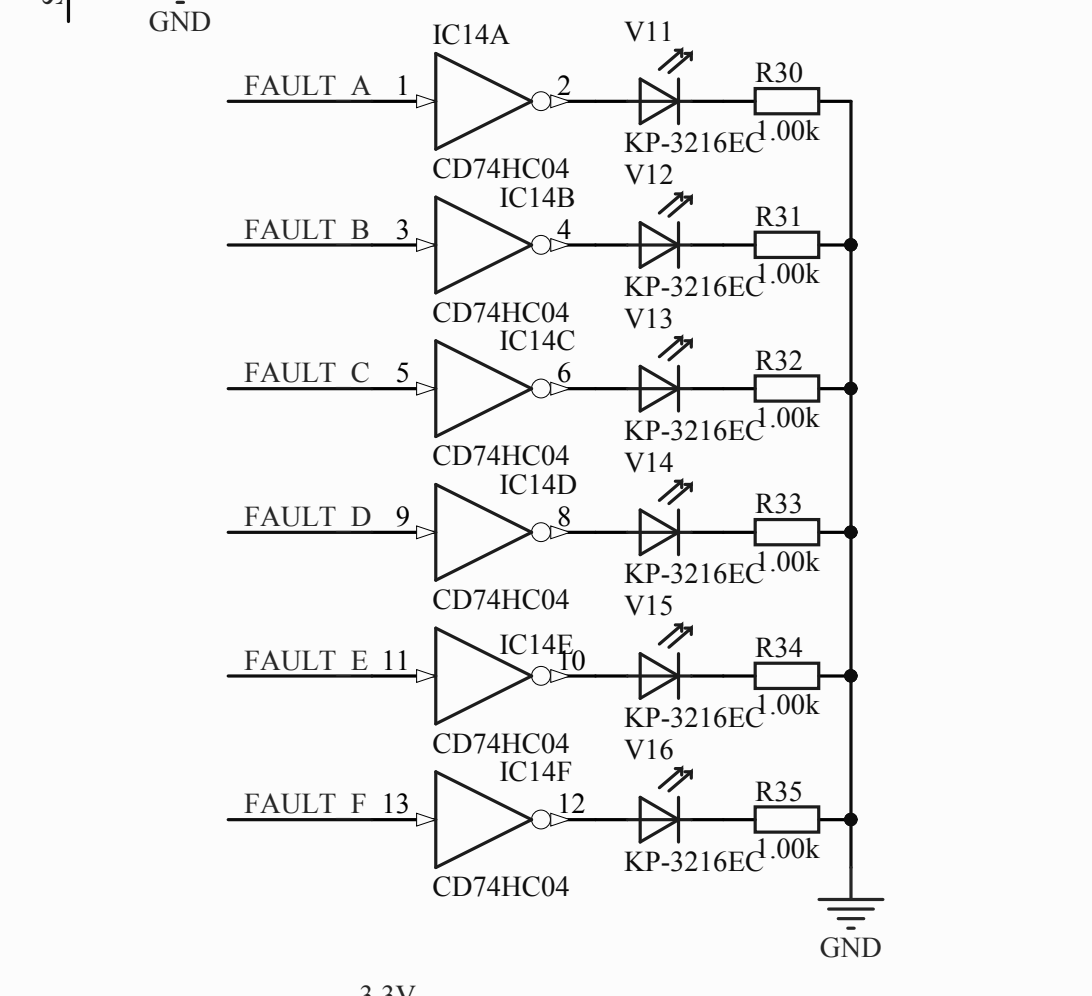
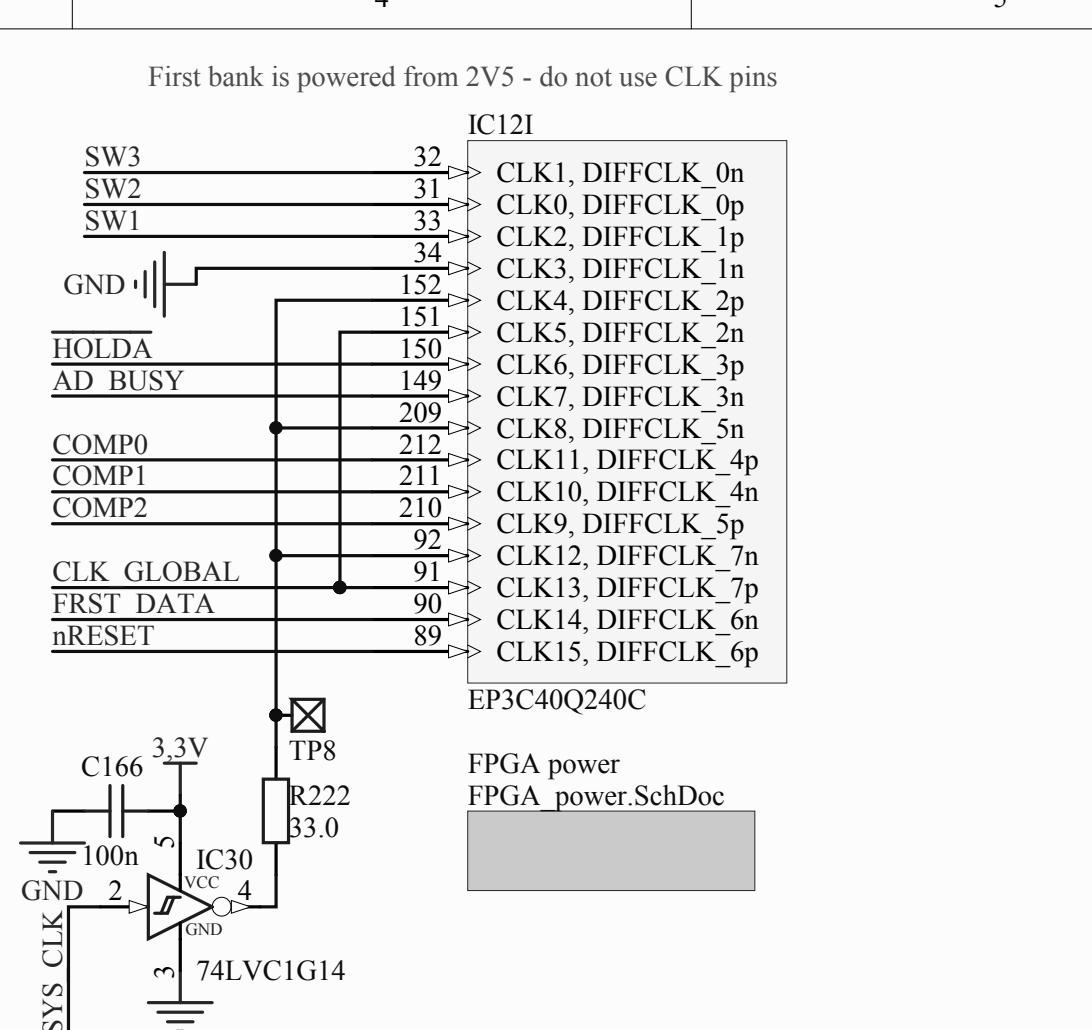
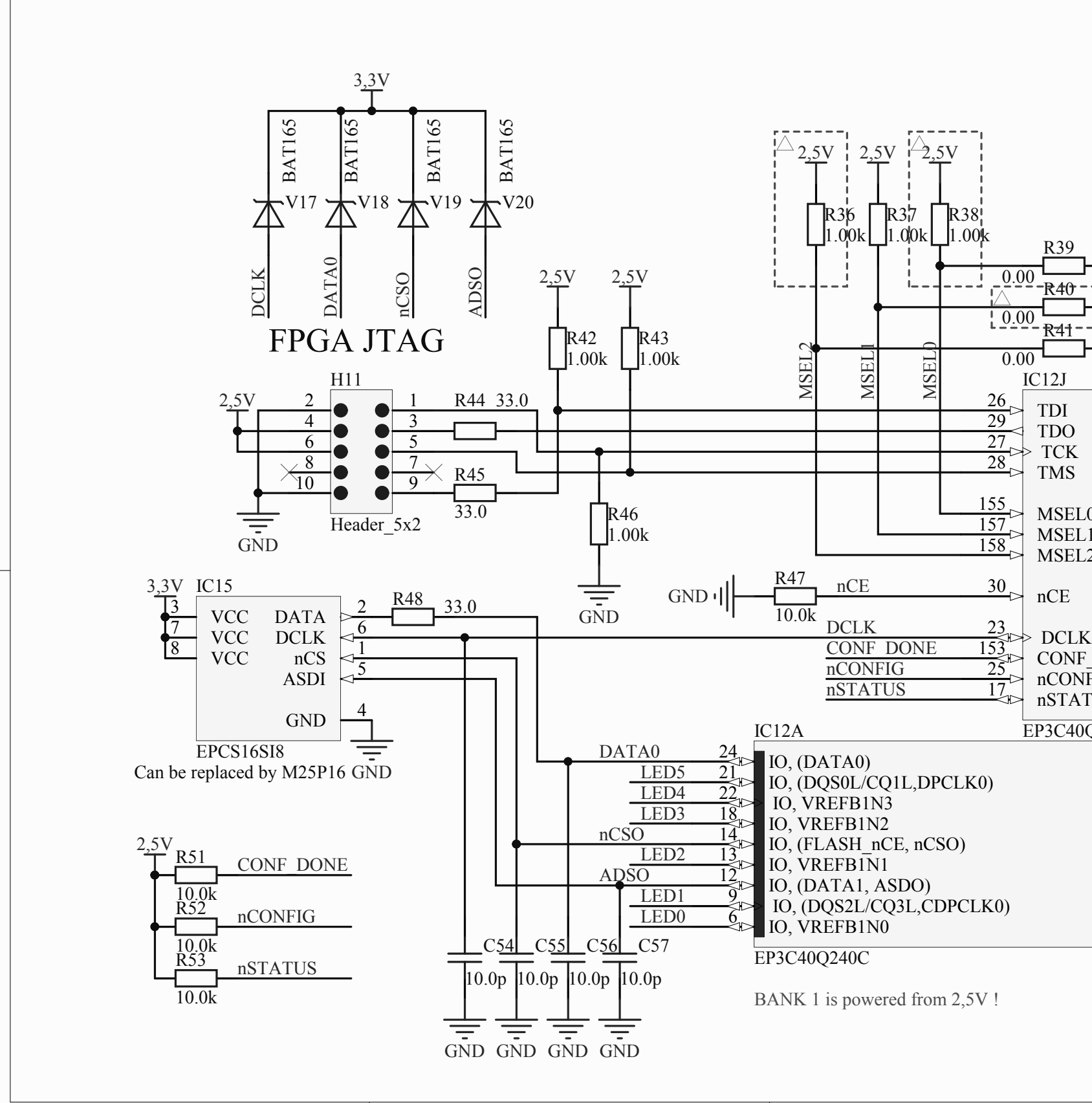
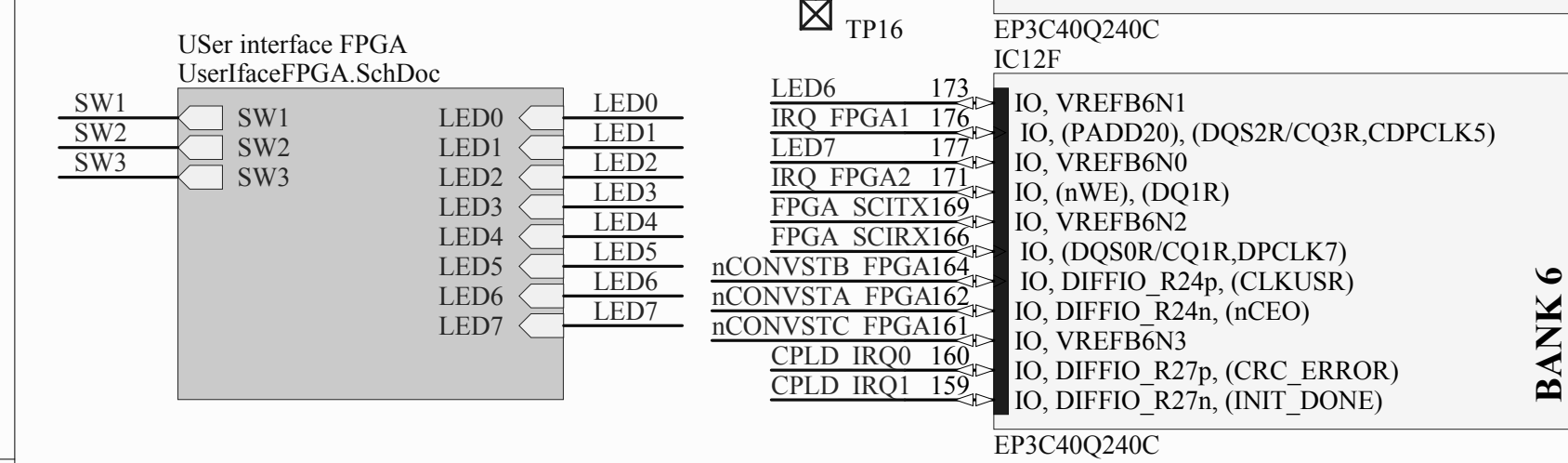
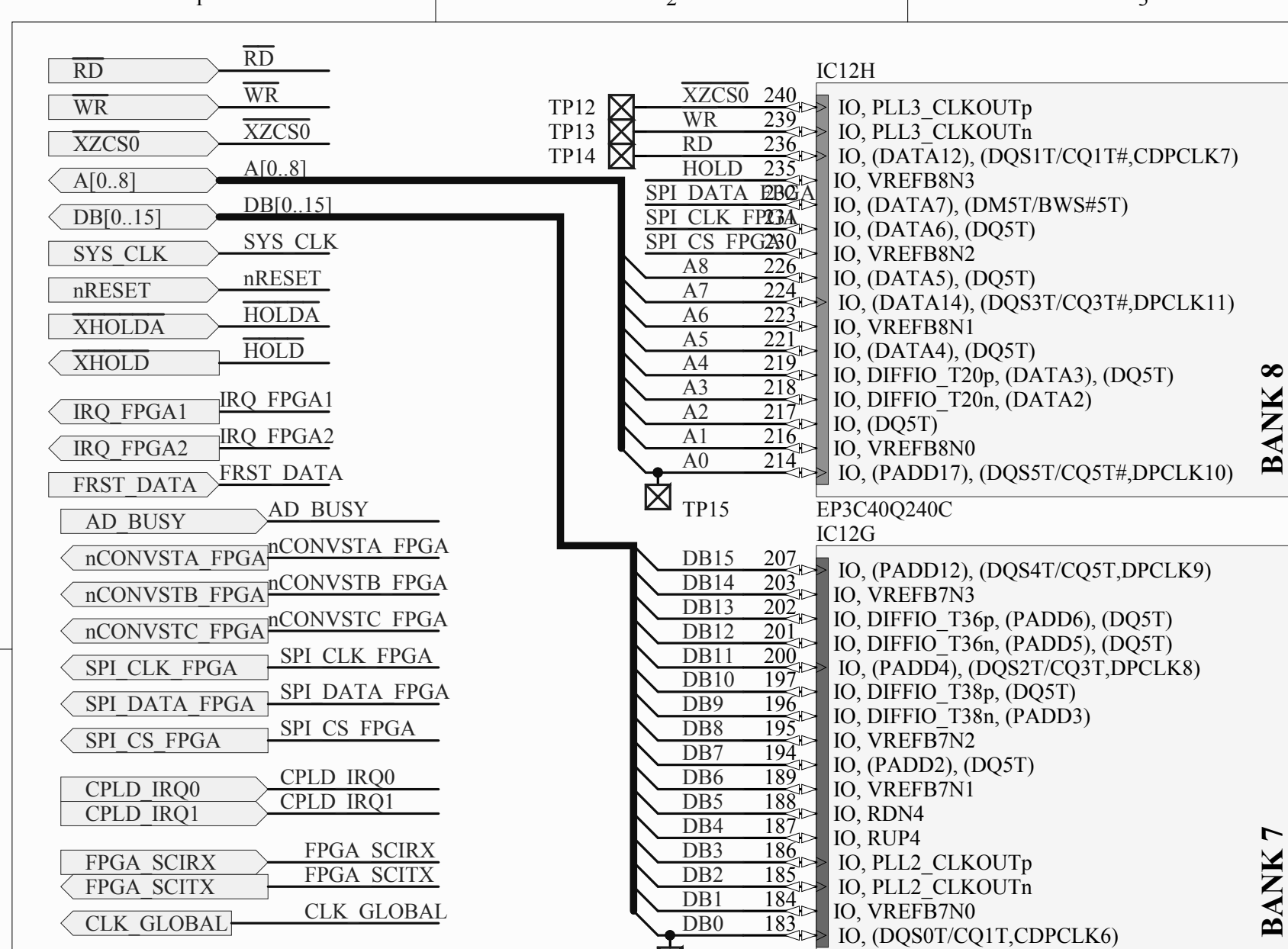
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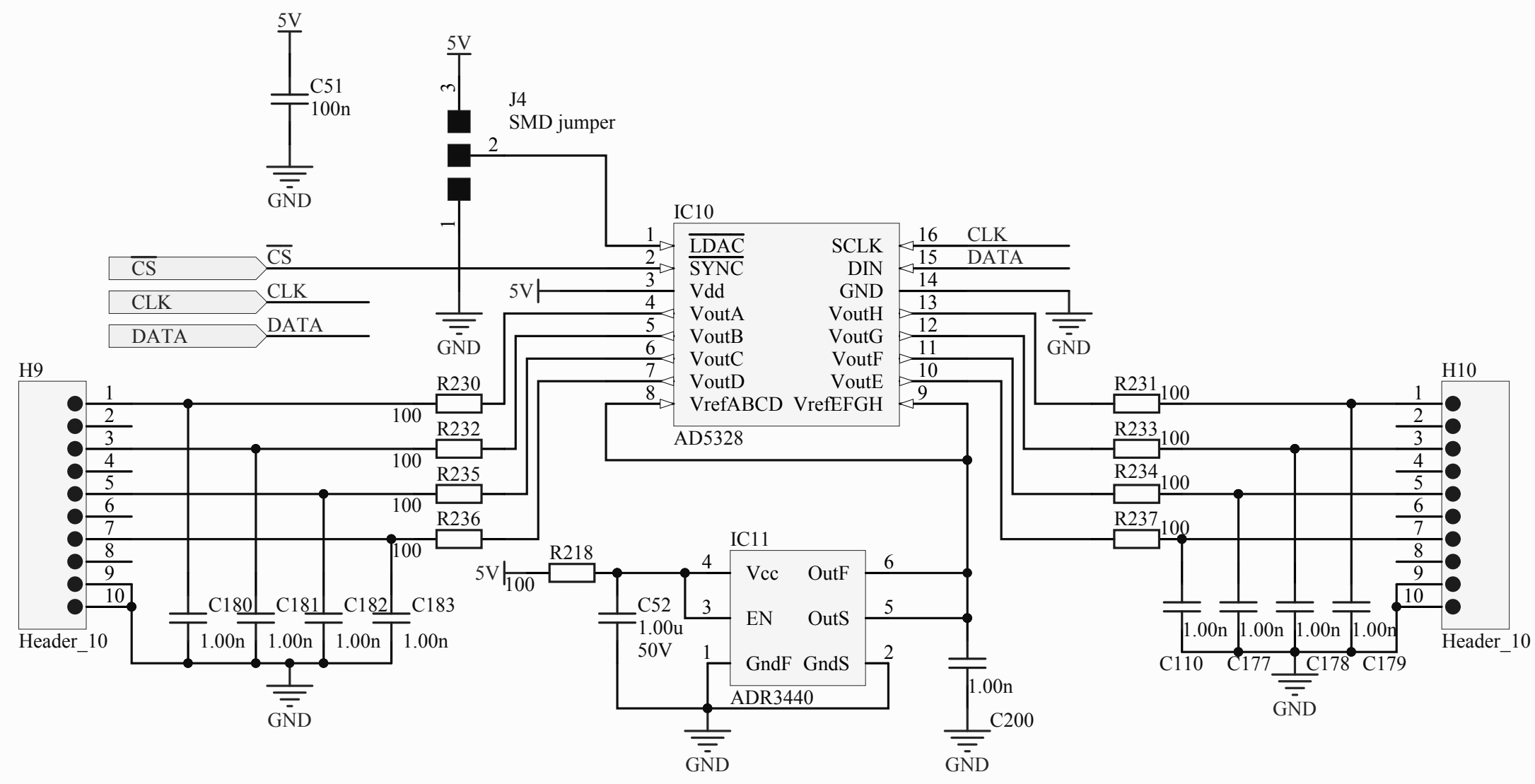
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	Author: Tomáš Košan	Subtitle: [SUBTITLE]		
	Checked by: LiPo, MaJa	Nr.: 1	Revision: 0.2	
	Approved by: Z. Peroutka	Type: typ	Sheet 1 of 1	
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 Regional Innovation Centre for Electrical Engineering Univerzitni 26 306 14 Plzen Czech Republic	Size: A4	Date: 5.8.2014	Title: SCH_title	
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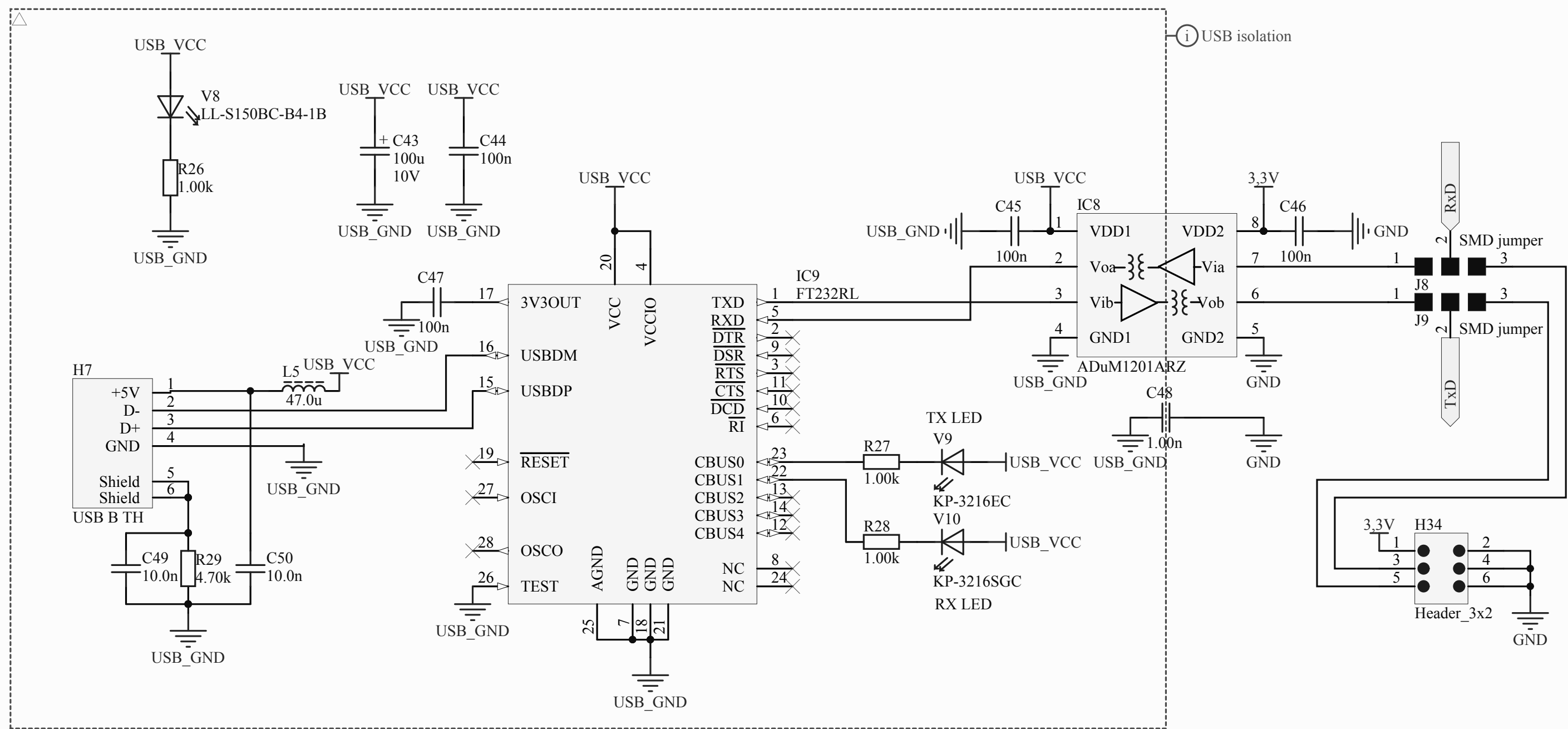


 Regional Innovation Centre for Electrical Engineering Univerzitni 26 306 14 Pízen Czech Republic	Size: A3	Date: 5.8.2014	Title: MLC interface	
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File: FPGA_part.SchDoc		Note: Data in fields enter via project/document parameters.		



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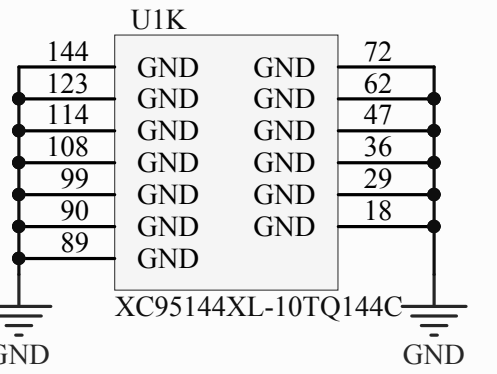
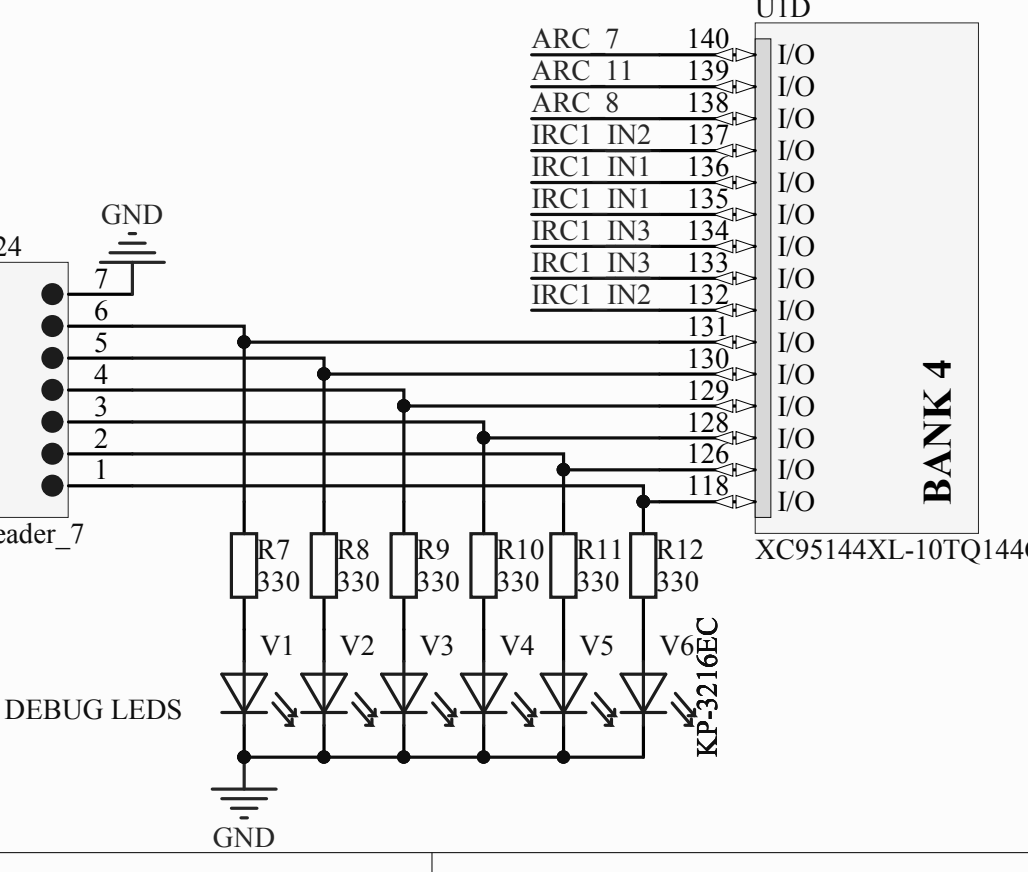
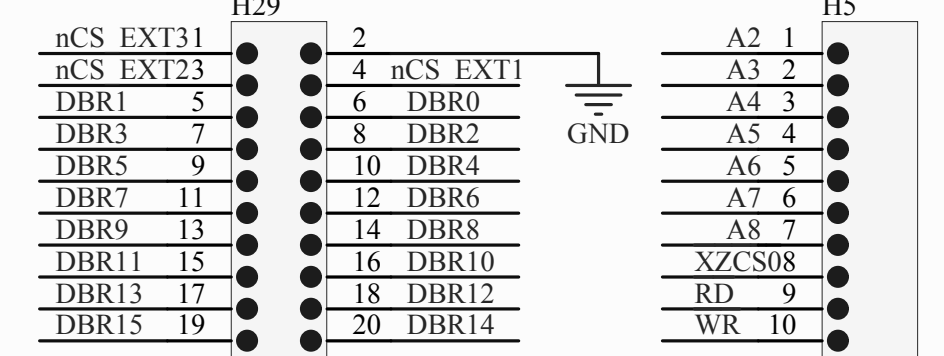
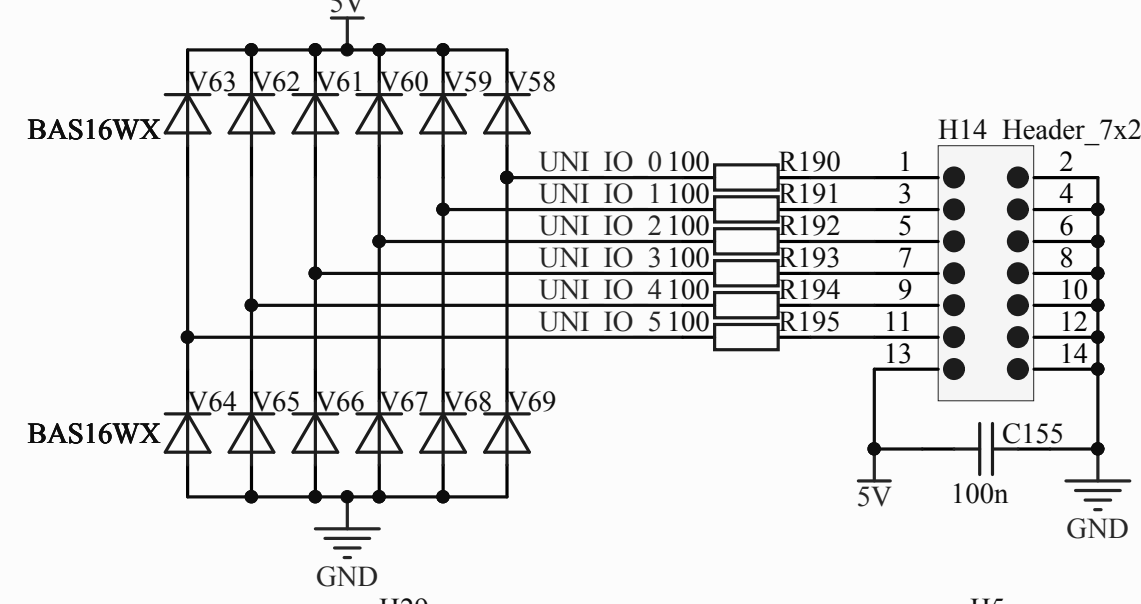
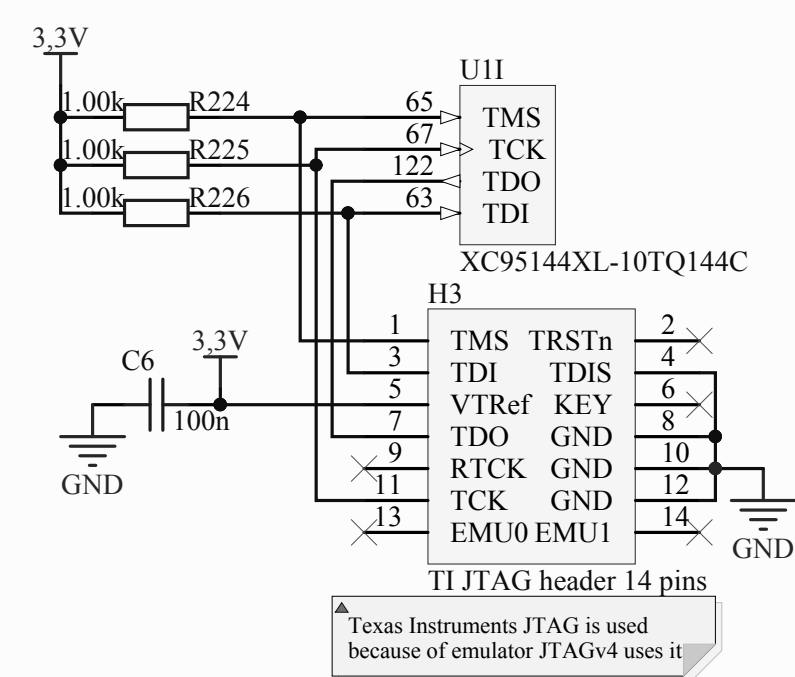
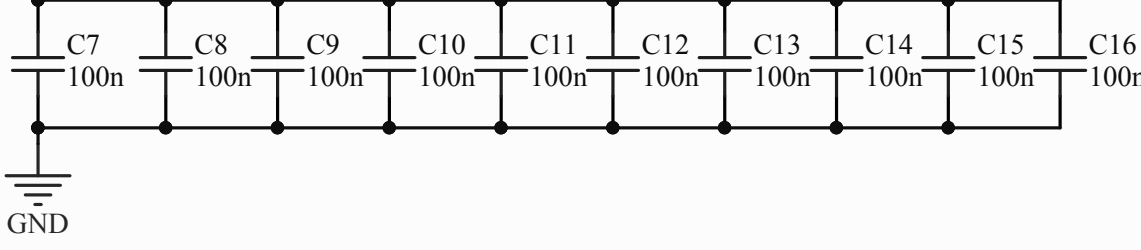
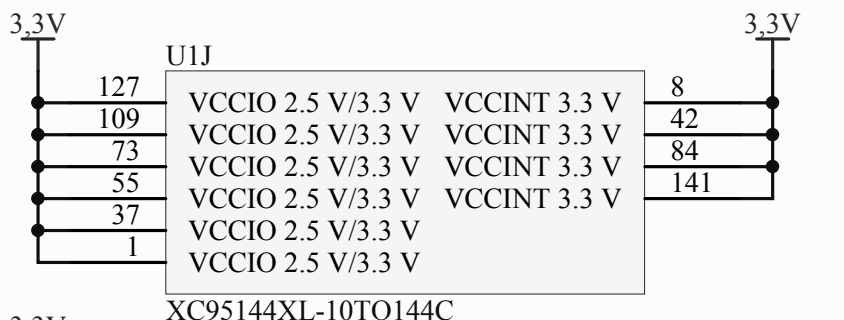
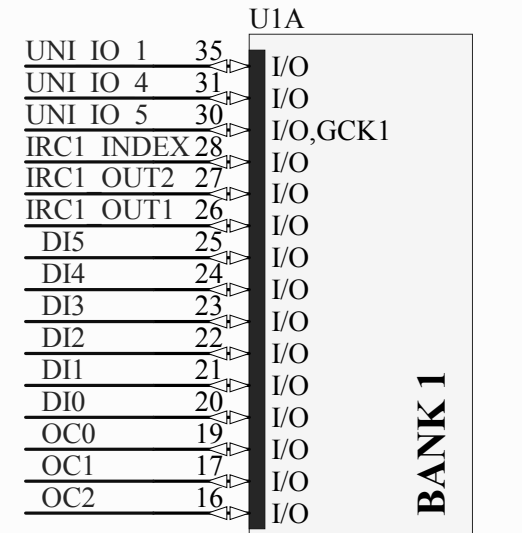
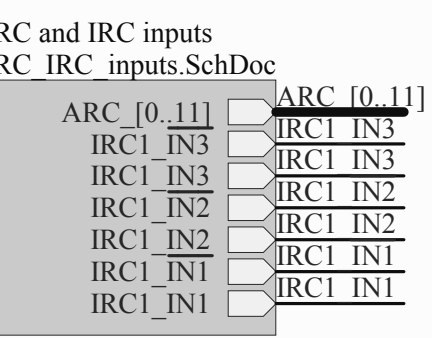
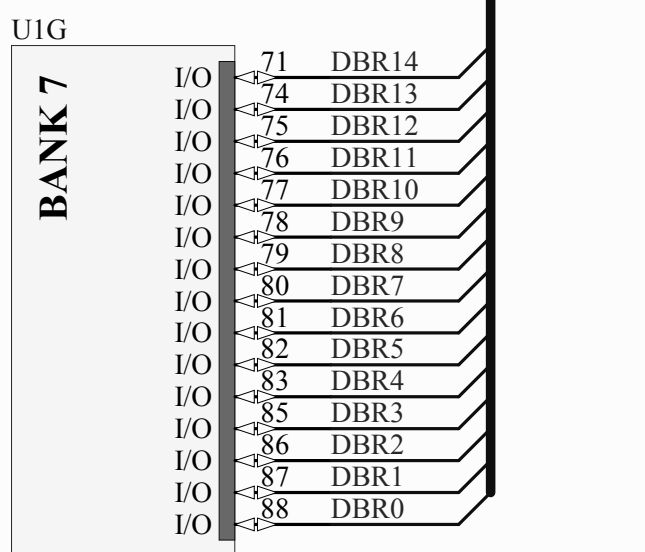
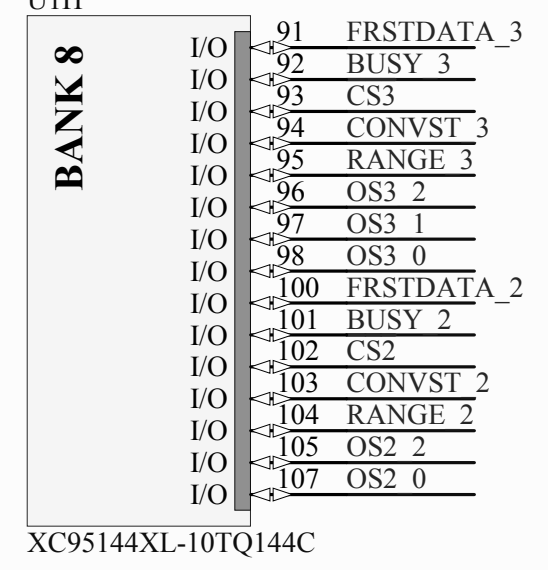
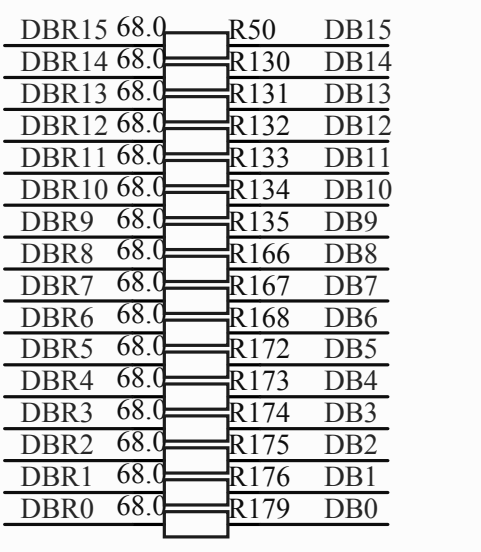
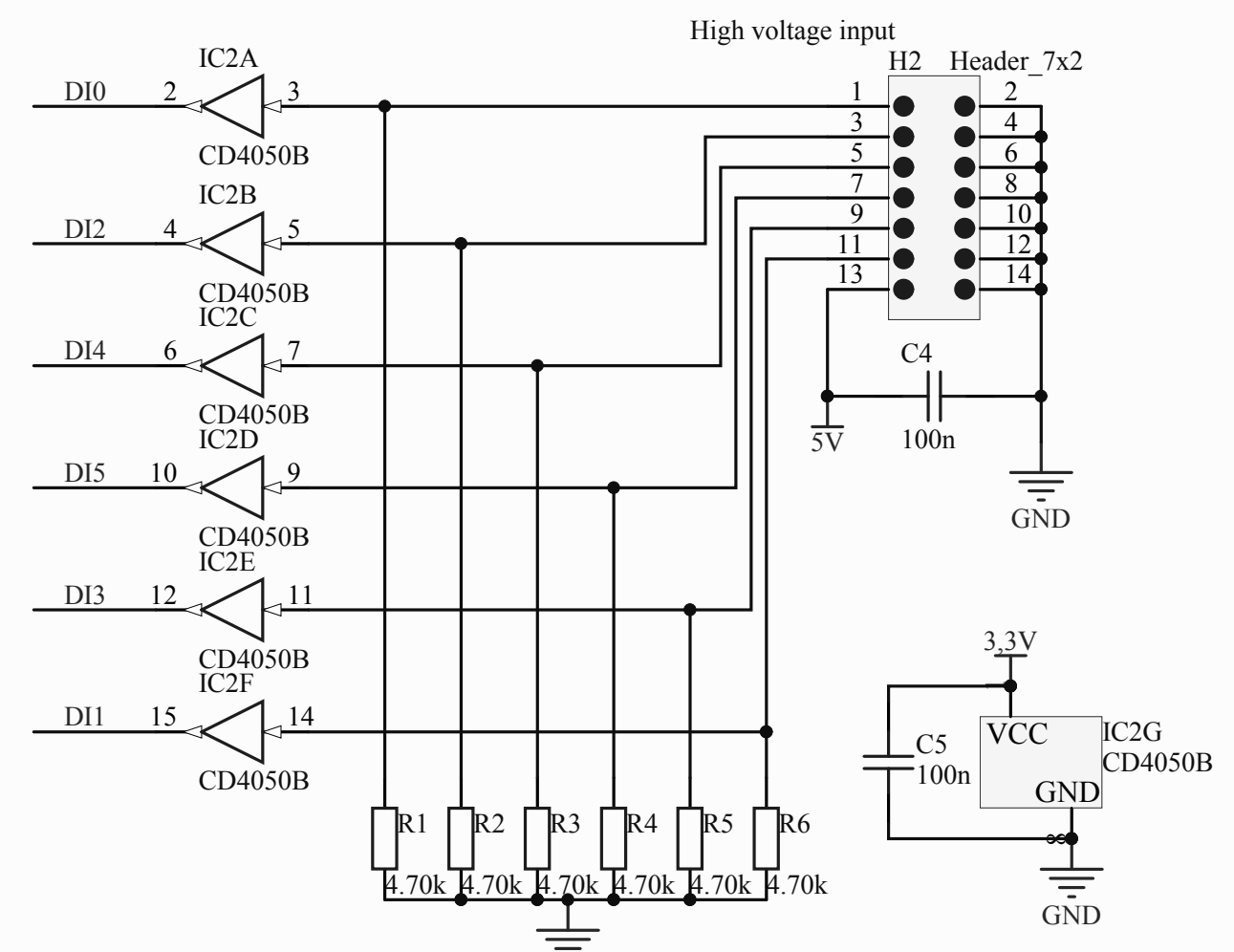
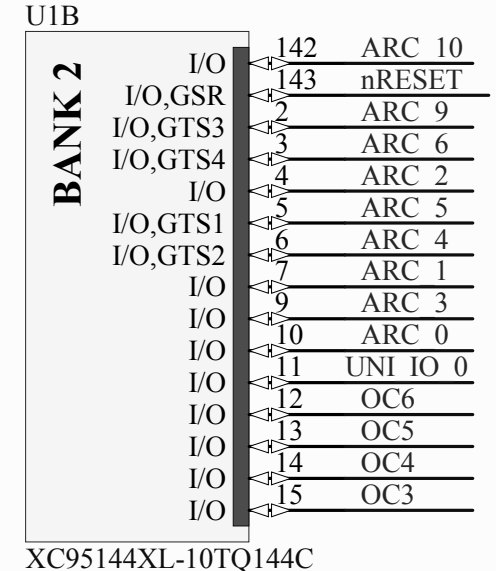
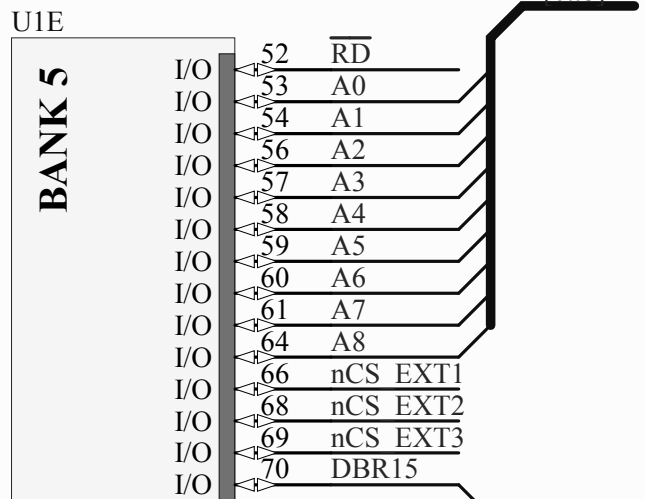
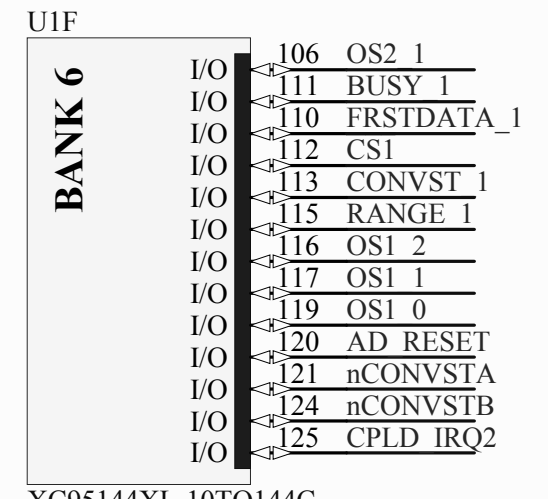
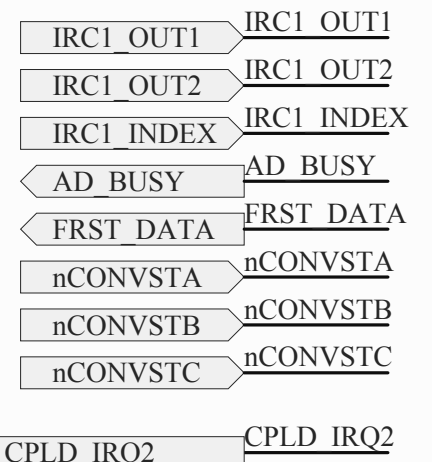
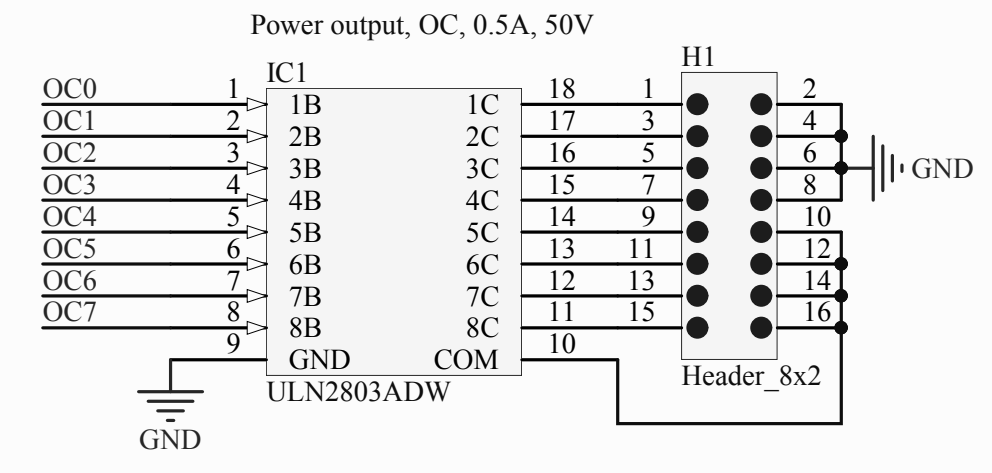
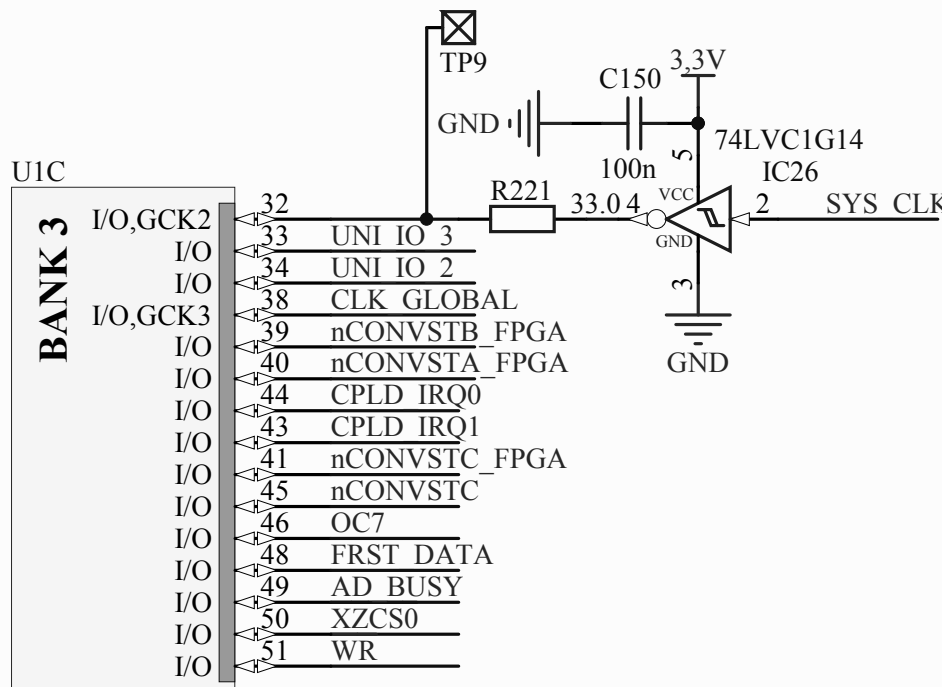
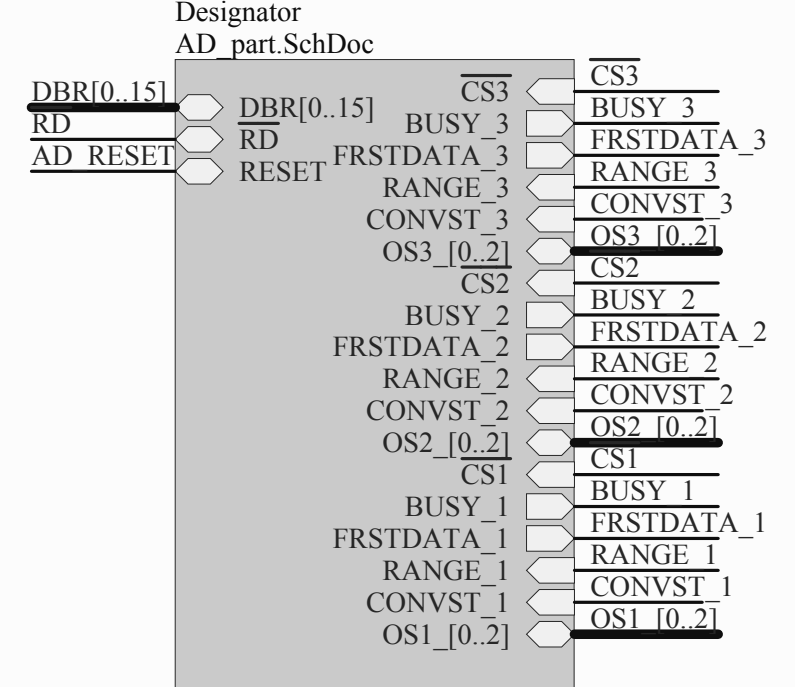
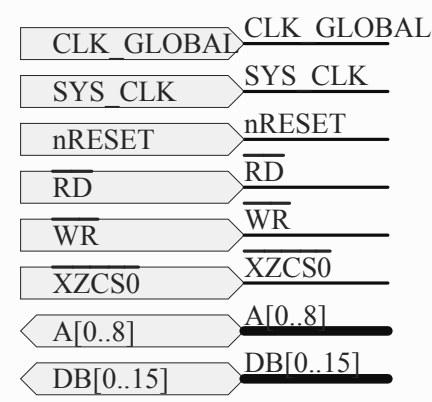
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File: DA_part.SchDoc			




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Approved by: Z. Peroutka	Type: typ	Sheet 1 of 1	
File: USB_SERIAL.SchDoc			

Note: Data in fields enter via project/document parameters.

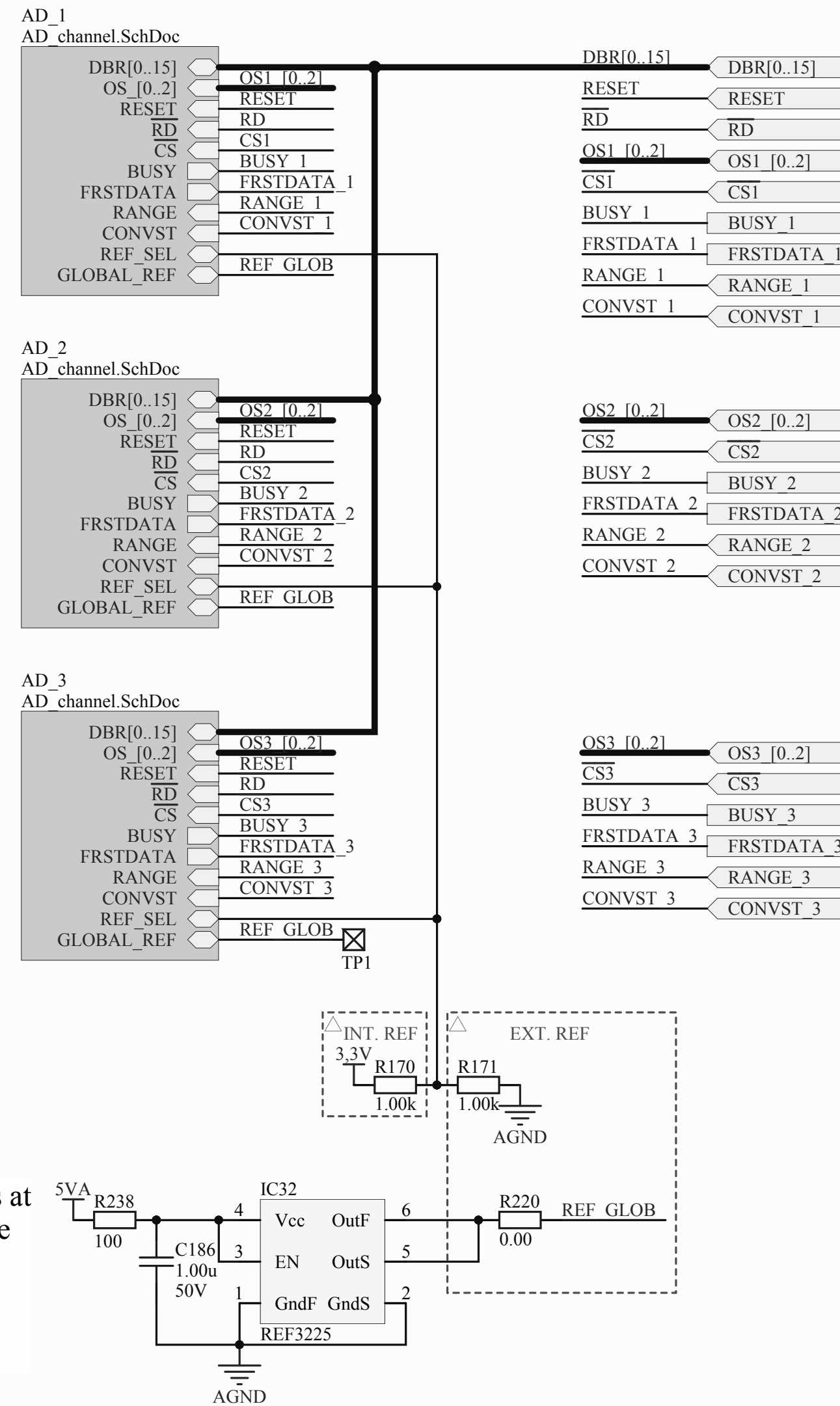




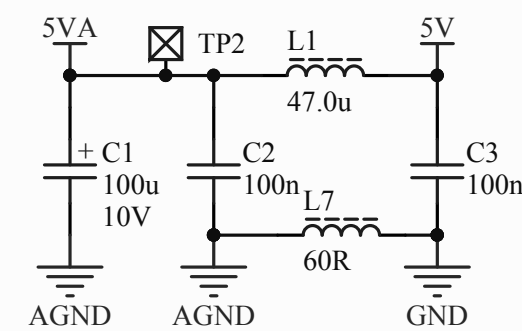
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Size: A3	Date: 5.8.2014	Title: MLC interface	
Author: Tomas Kosan	Subtitle: [SUBTITLE]		
Checked by: [NAME]	Nr.: 1	Revision: [REVISION]	
Approved by: [NAME]	Type: [TYPE]	Sheet 1 of 1	
File: CPLD_part.SchDoc			

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Usable ADs are AD7606, AD7609, difference is at inputs, AD7609 has full differential inputs, while AD7606 does not.



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	Approved by: Z. Peroutka	Type: [TYPE]	Sheet 1 of 1	
	File: AD_part.SchDoc	Note: Data in fields enter via project/document parameters.		

GPIO20/CANTXB
GPIO21/CANRXB

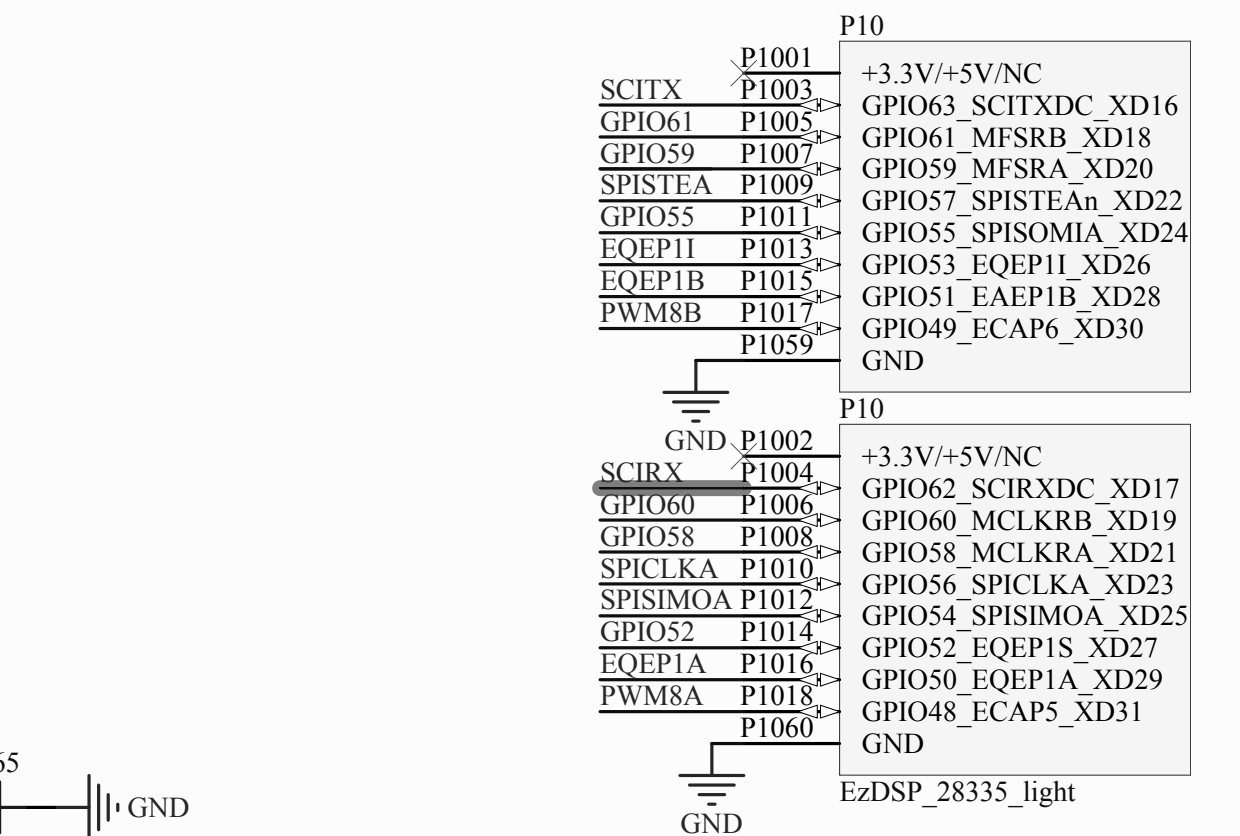
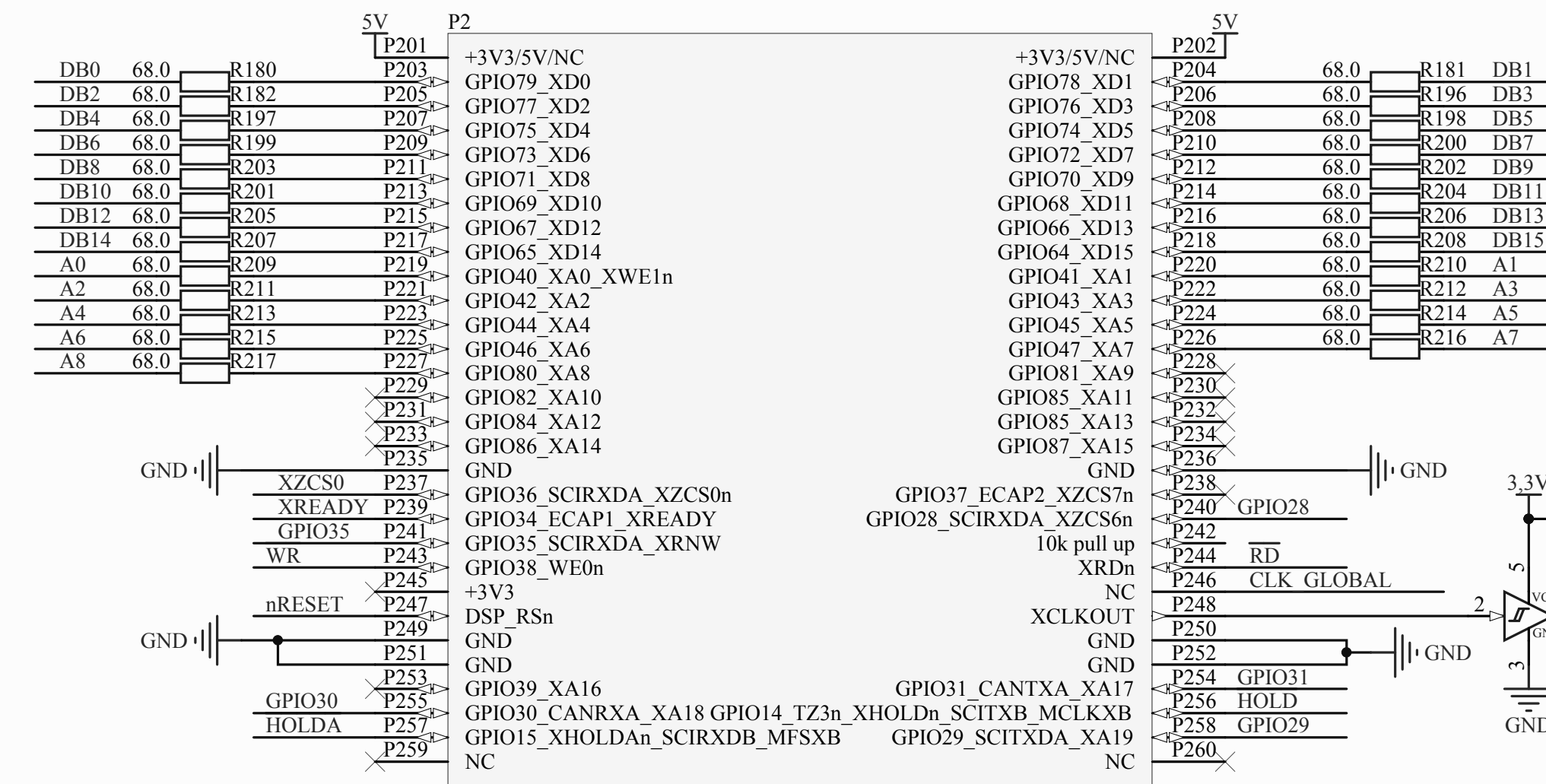
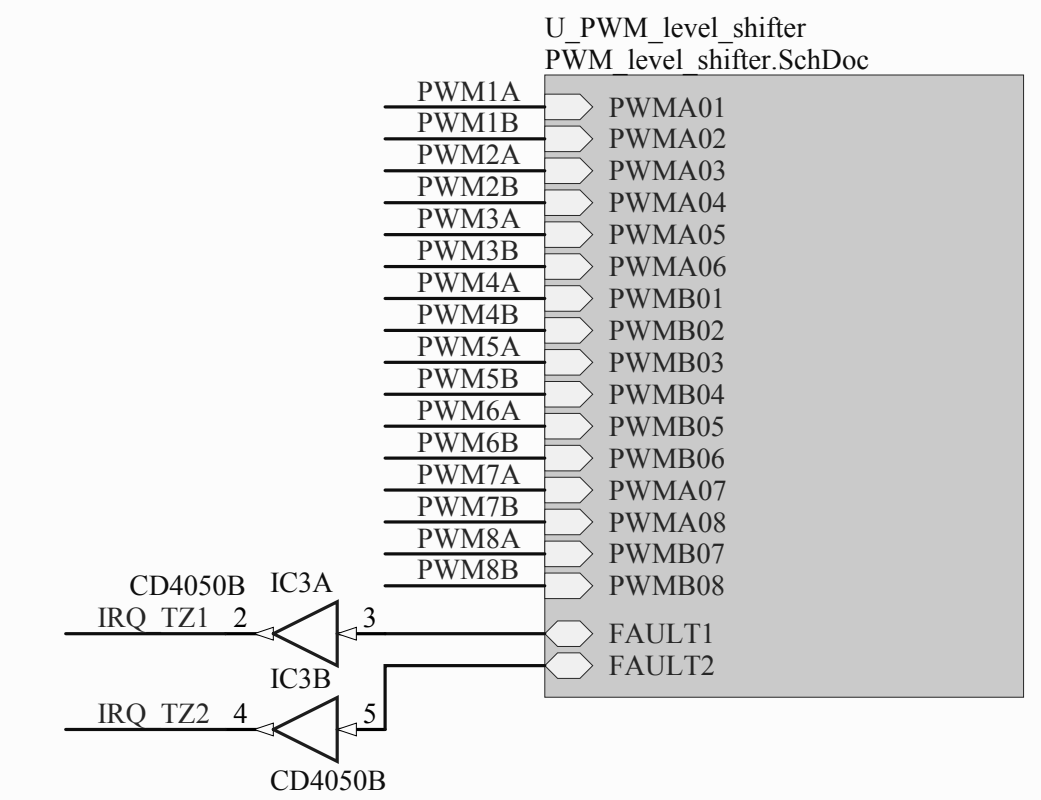
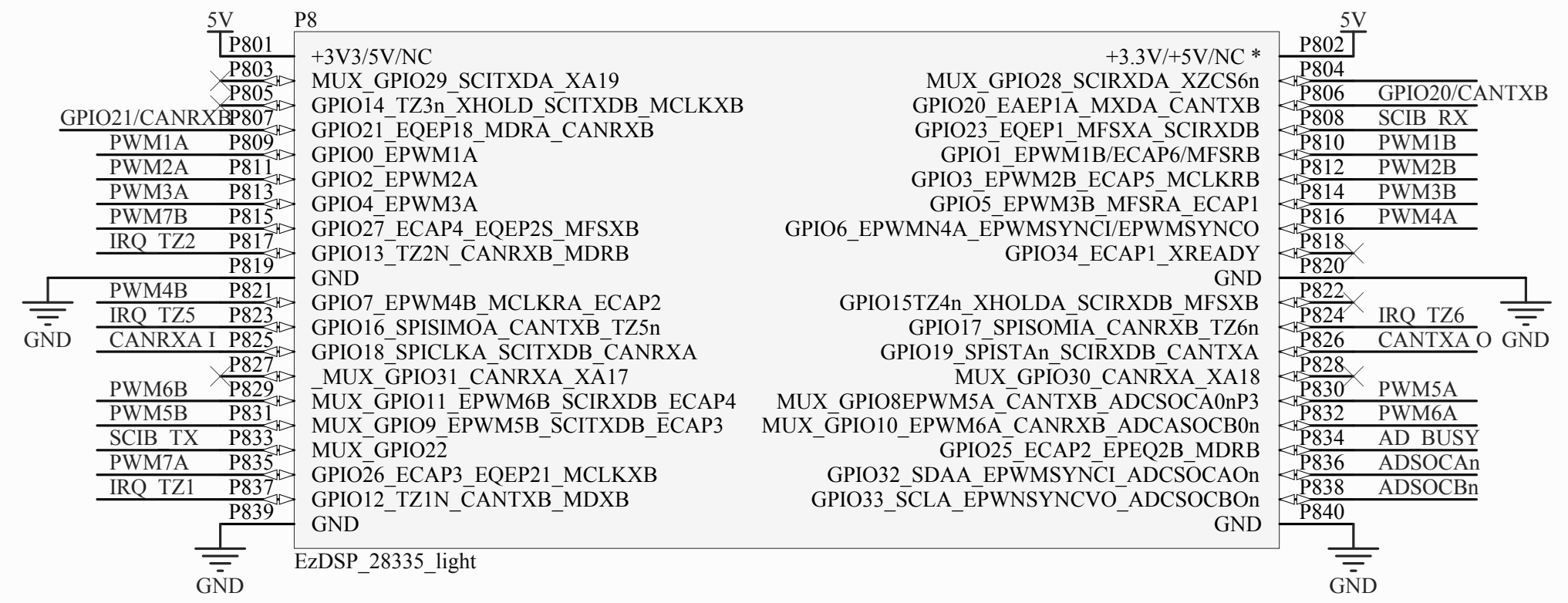
CANTXA CANTXA O
CANRXA CANRXA I

FRST DATA GPIO35

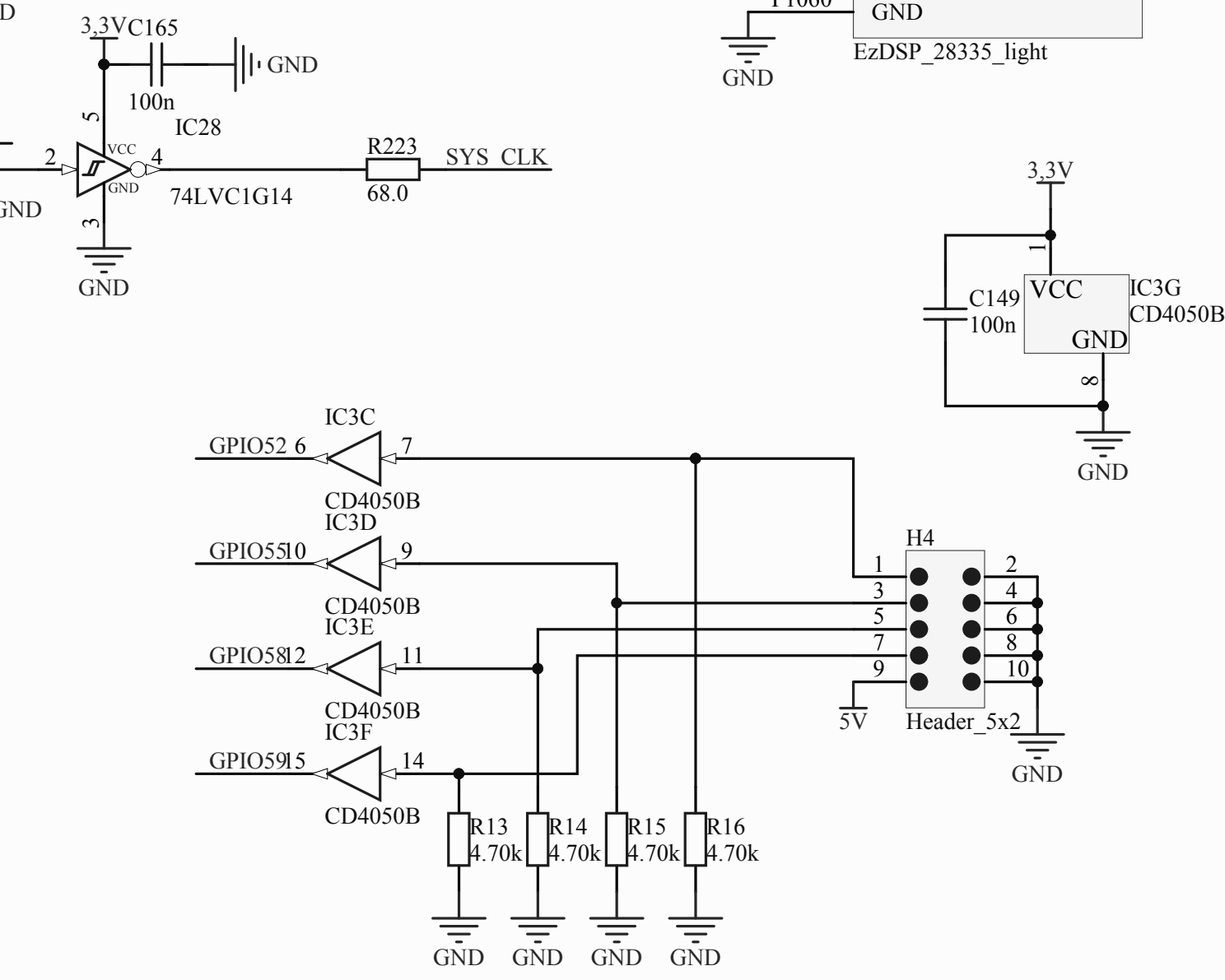
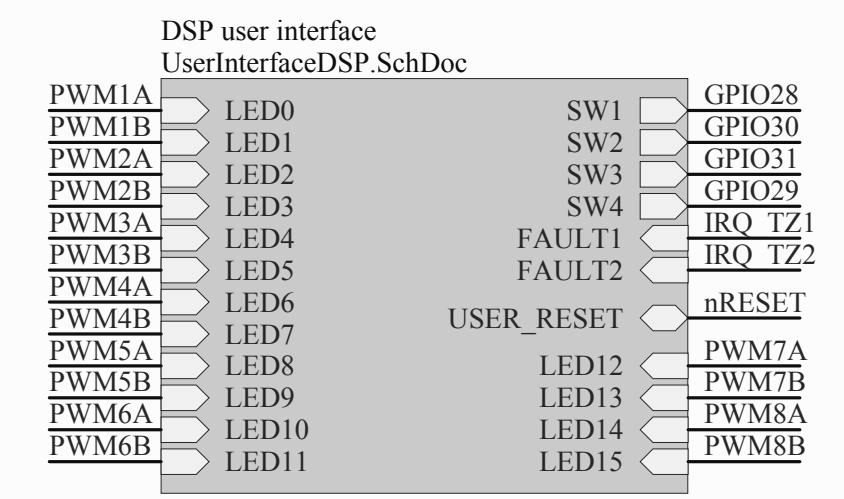
CPLD_IRQ2 GPIO60
nCONVSTC GPIO61


RD RD
WR WR
XZCS0 XZCS0
A[0..8] A[0..8]
DB[0..15] DB[0..15]
SYS_CLK SYS_CLK
nRESET nRESET
XHOLDA HOLDA
XHOLD HOLD
SCITX SCITX
SCIRX SCIRX
SPISTEA SPISTEA
SPICLKA SPICLKA
SPISIMOA SPISIMOA
IRC1_IN1 EQEP1A
IRC1_IN2 EQEP1B
IRC1_INDEX EQEP1I
nCONVSTA ADSOCA n
nCONVSTB ADSOCB n
IRQ_TZ5 IRQ_TZ5
IRQ_TZ6 IRQ_TZ6
AD_BUSY AD_BUSY

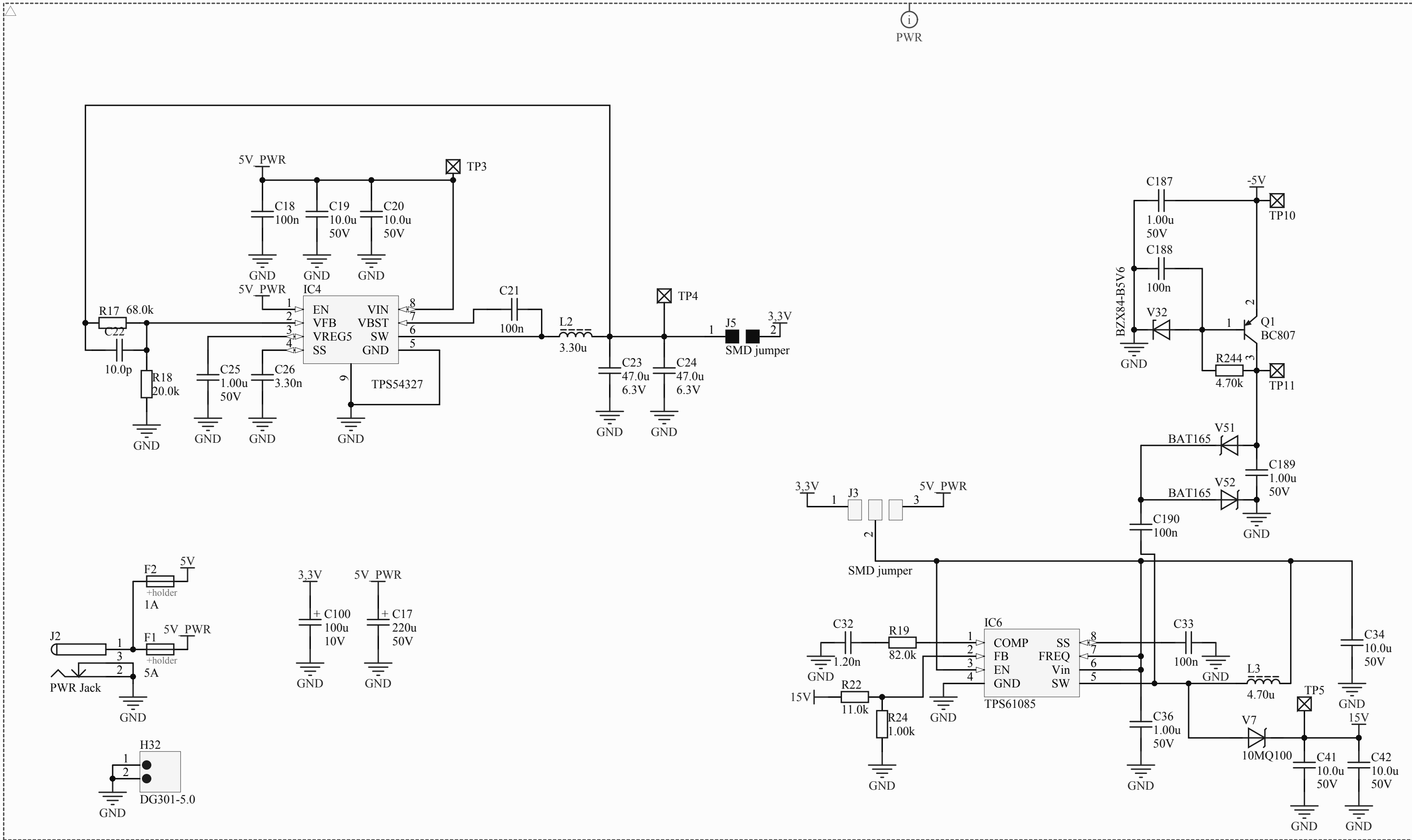
CLK GLOBAL CLK GLOBAL



Address bus is used in range A0 to A16 for RAM. Peripherals uses A0 to A11.



 Regional Innovation Centre for Electrical Engineering Univerzitni 26 306 14 Plzen Czech Republic	Size: A3	Date: 5.8.2014	Title: MLC interface	
	Author: [NAME]	Subtitle: [SUBTITLE]		
	Checked by: [NAME]	Nr.: 1	Revision: [REVISION]	
	Approved by: [NAME]	Type: [TYPE]	Sheet 1 of 1	
File: eZdsp_335_mapping_SchDoc		Note: Data in fields enter via project/document parameters.		

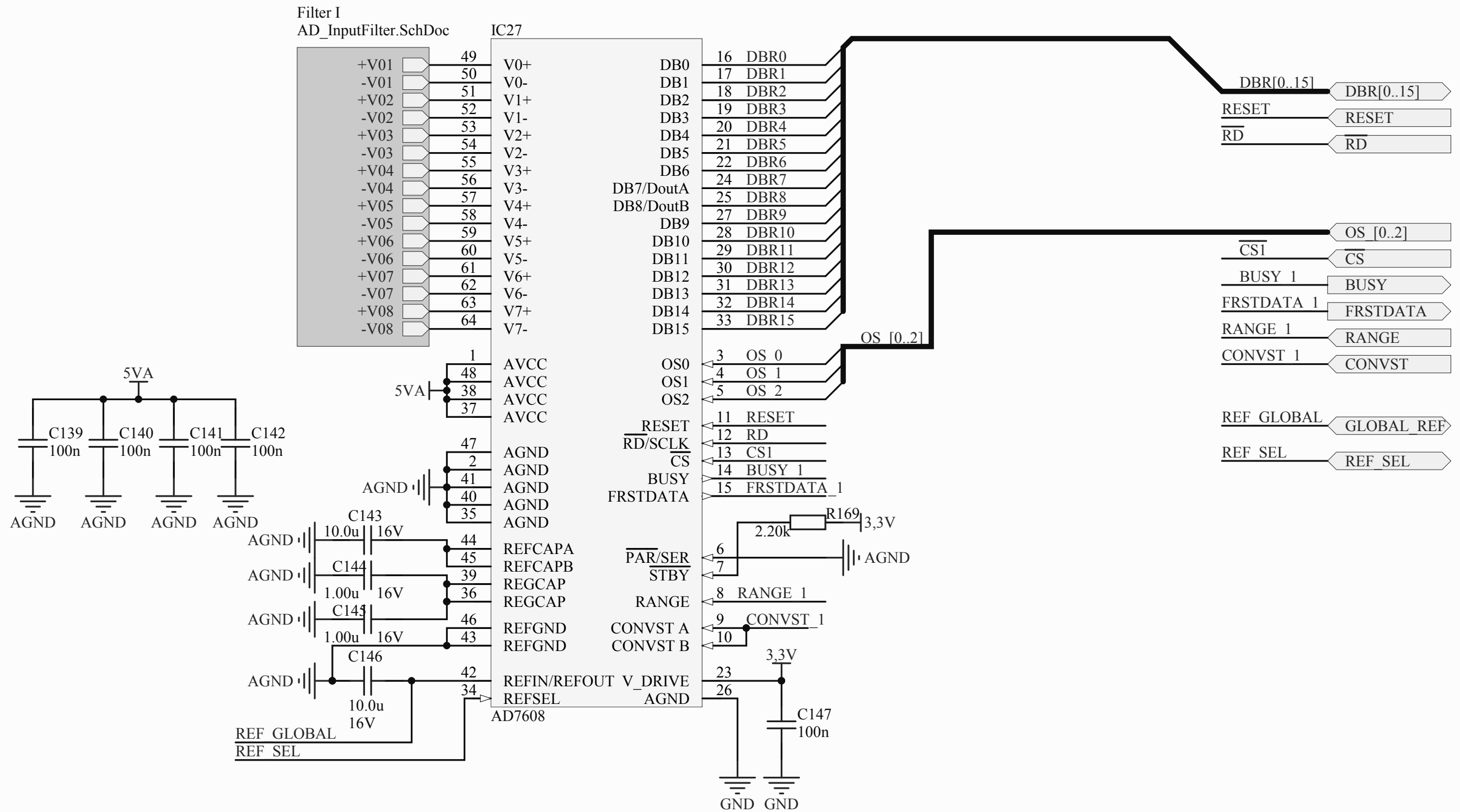


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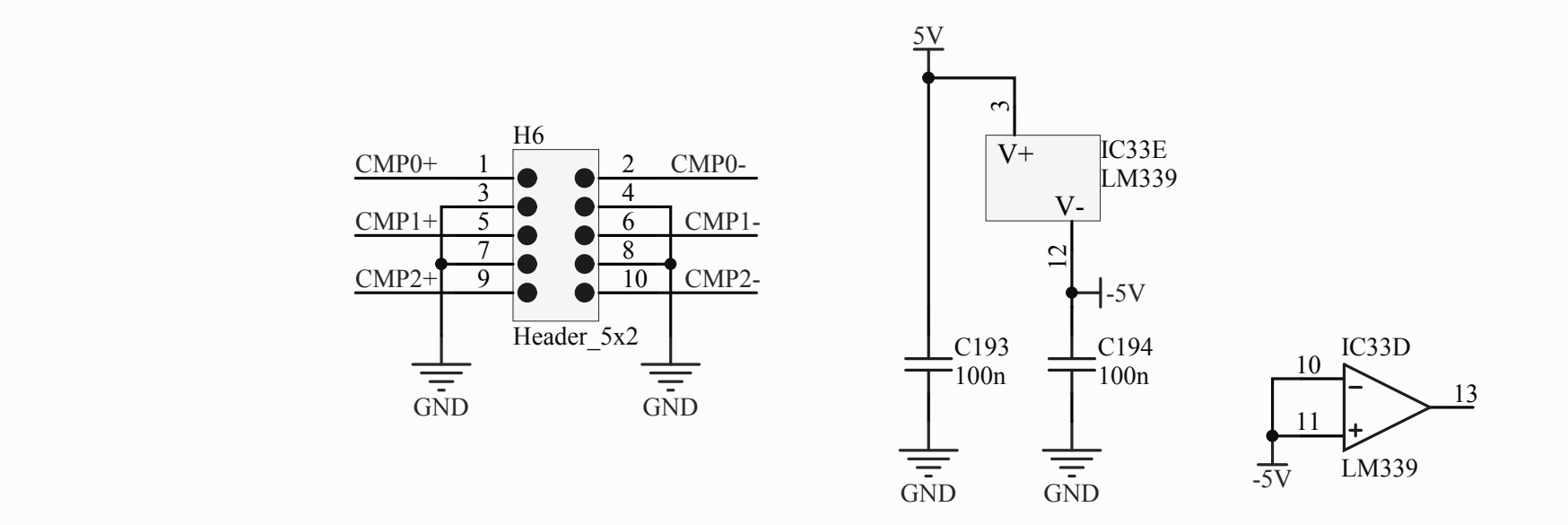
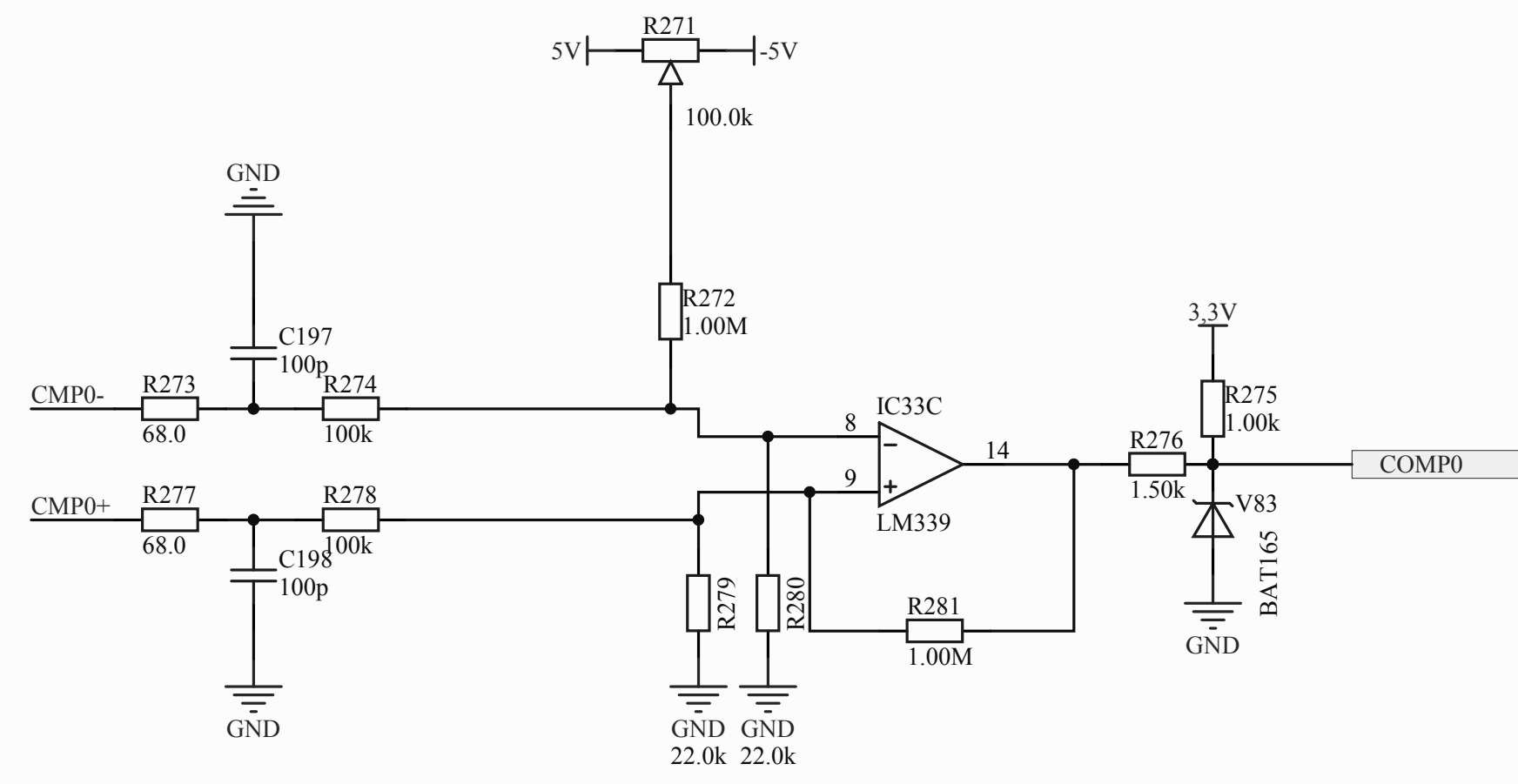
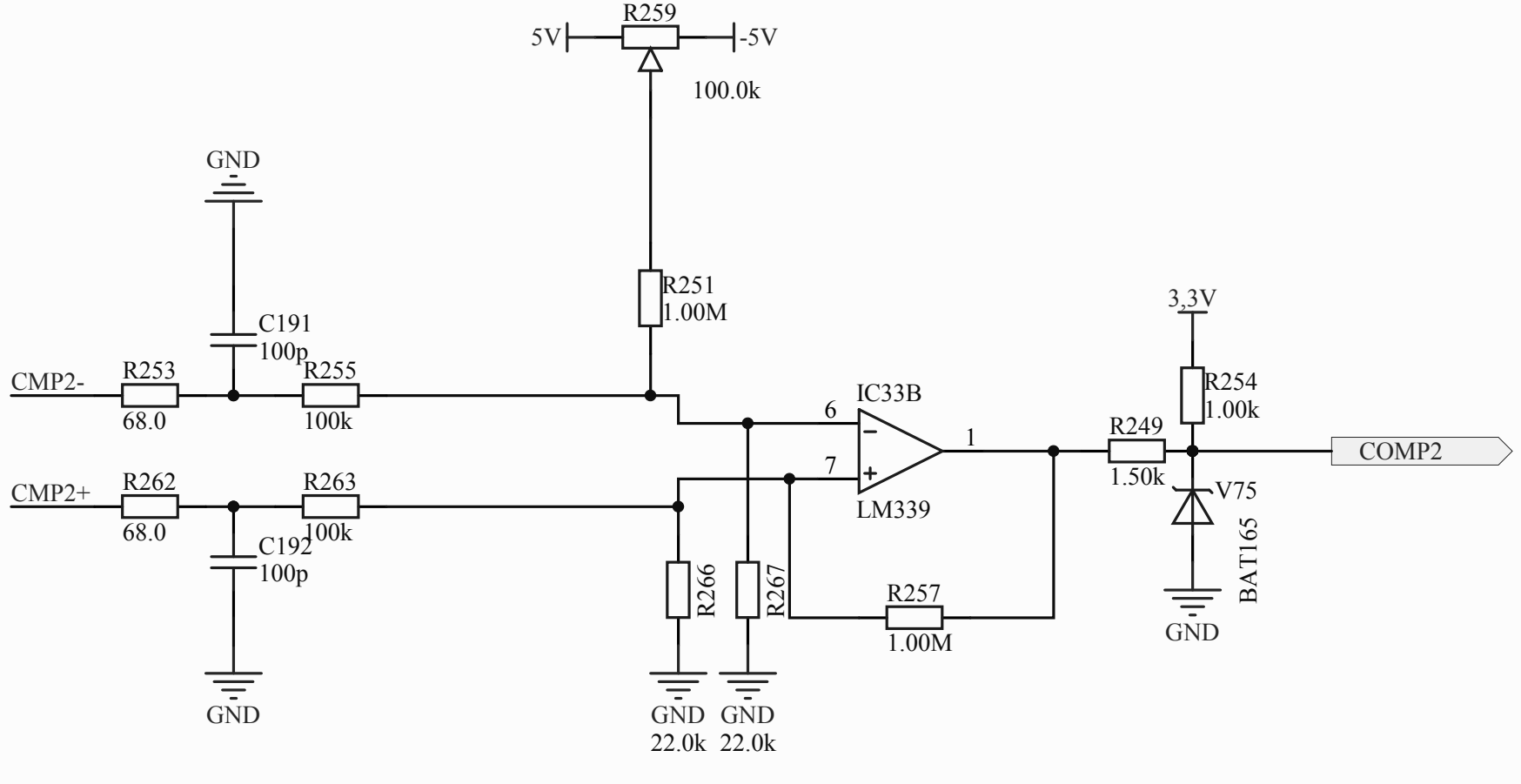
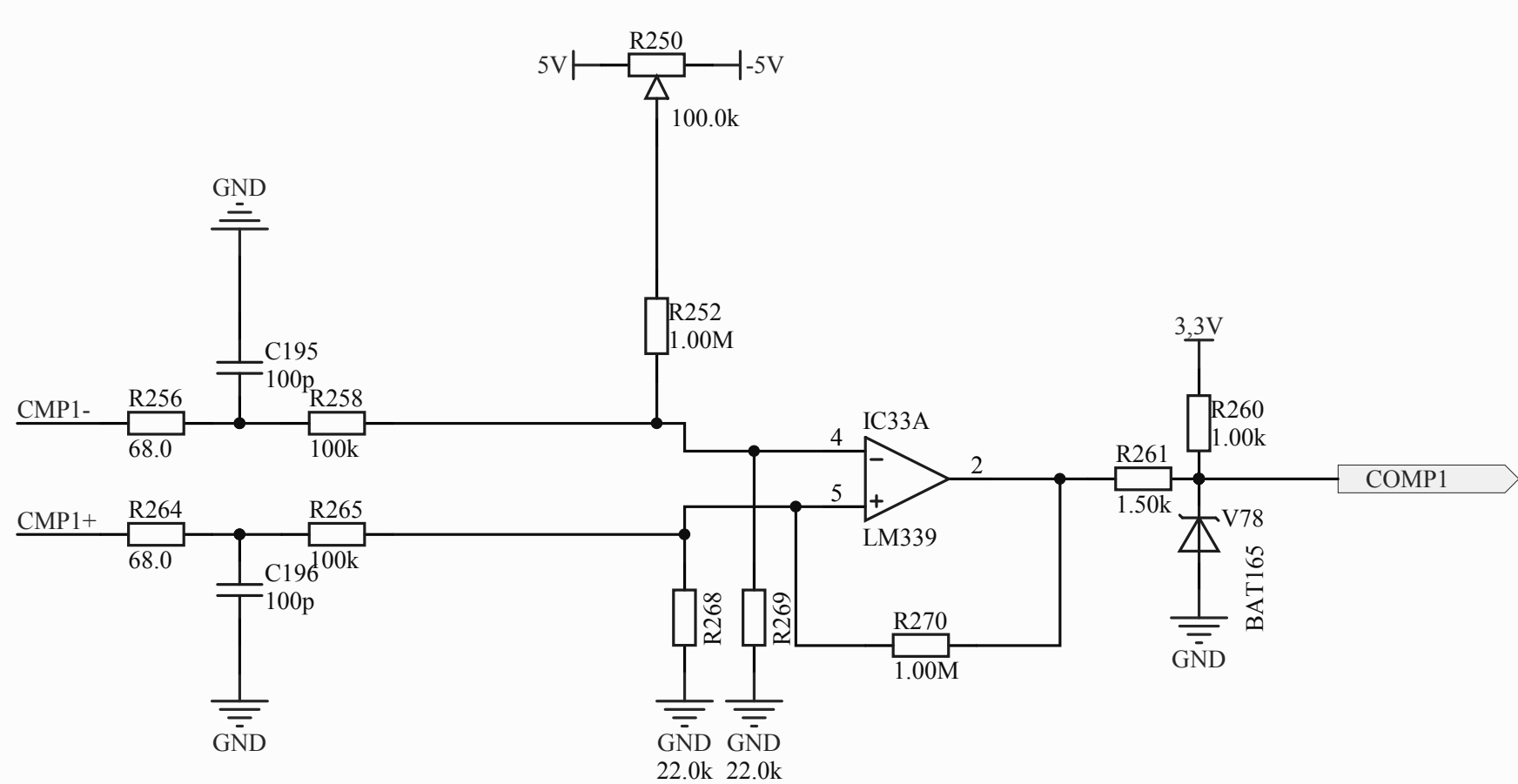
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Date: 5.8.2014
Author: Tomáš Košan
Checked by: LiPo, MaJa
Approved by: Z. Peroutka

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Nr.: 1
Type: typ
File: power_source.SchDoc
Revision: 0.2
Sheet 1 of 1

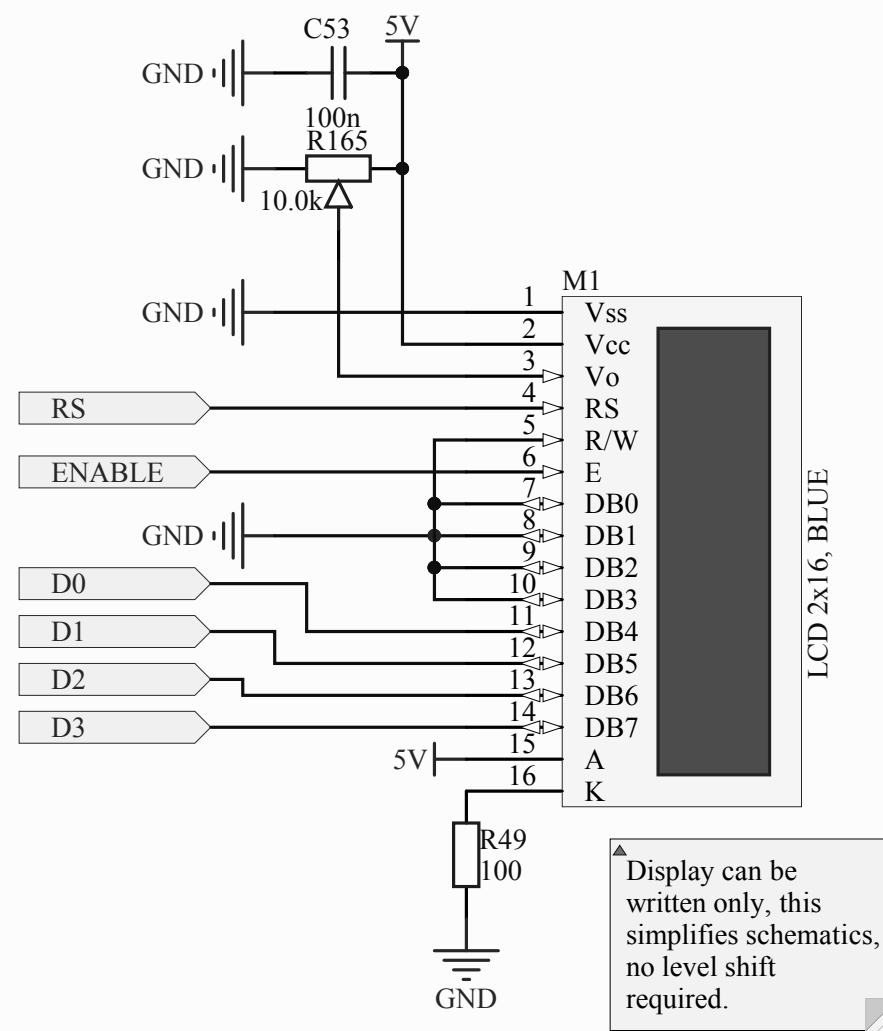
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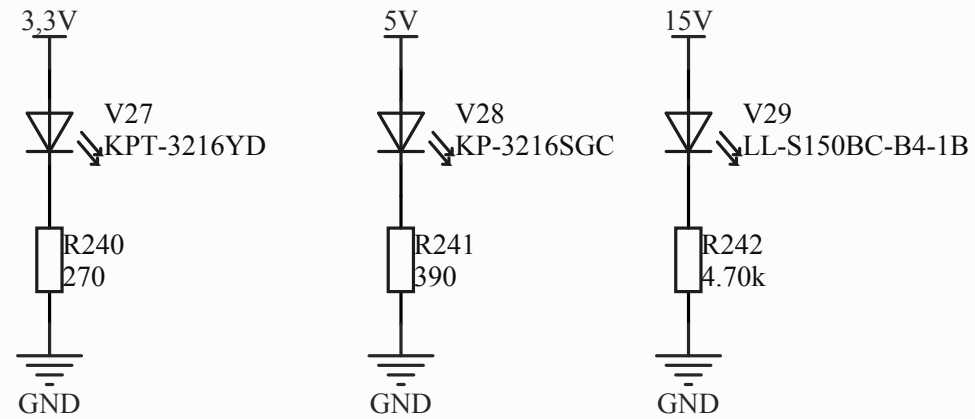


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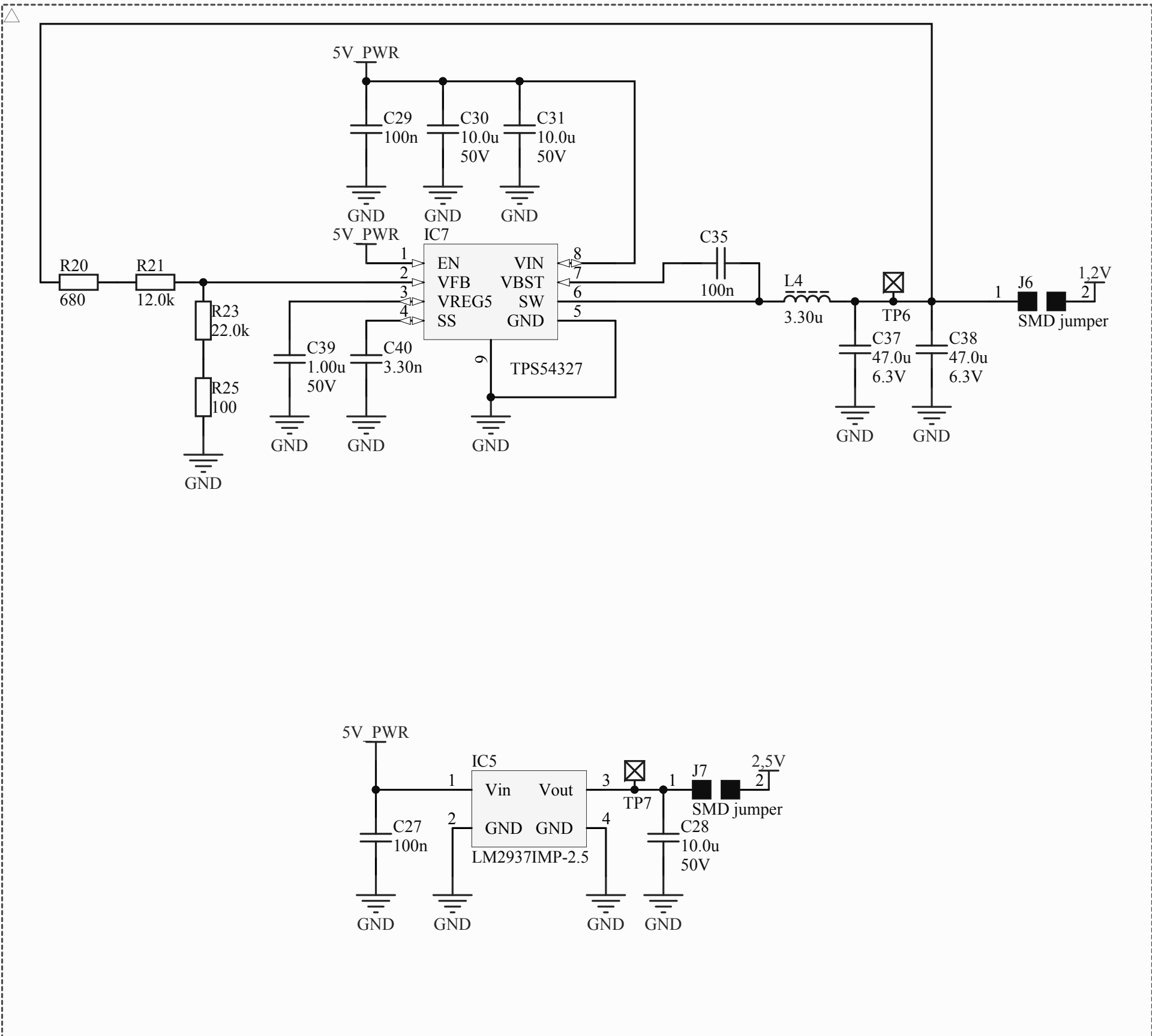
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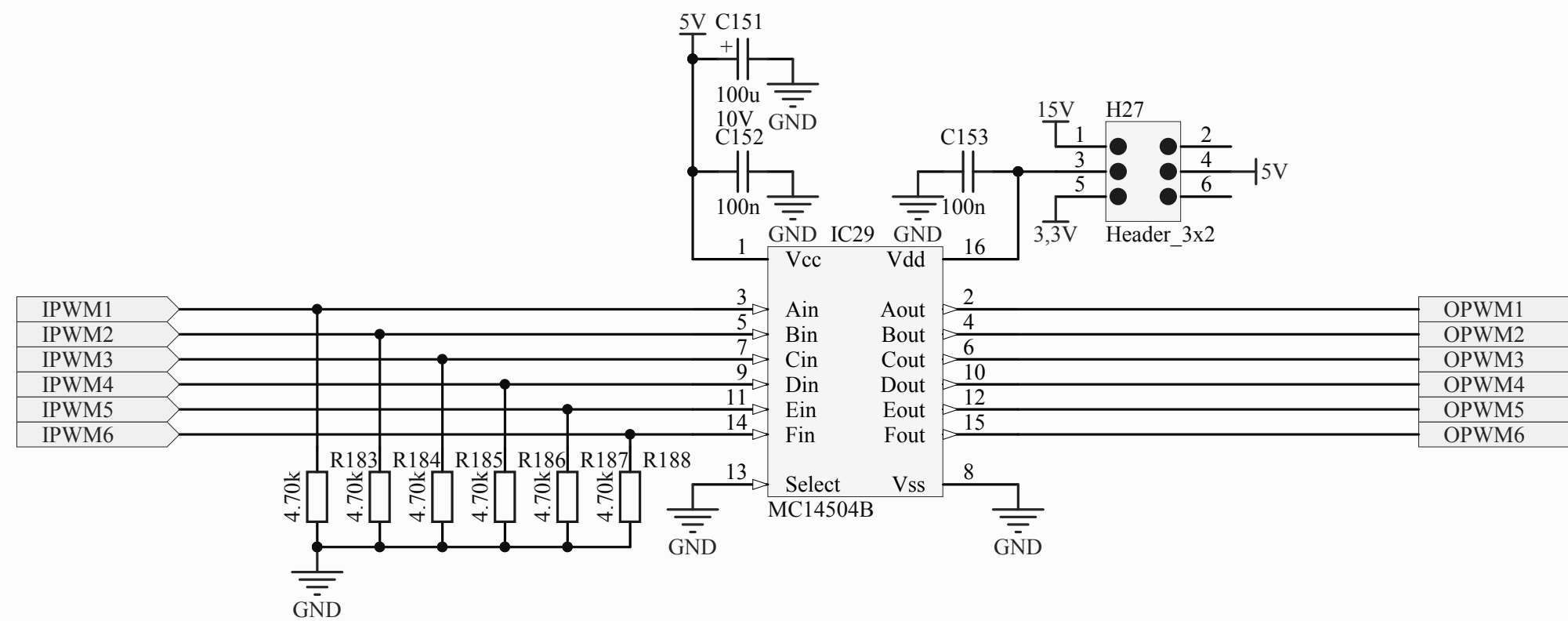
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i FPGA PWR



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Approved by: Z. Peroutka	Type: typ	Sheet * of *	
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